must be able to survive in the radiation environment of space, since radiation can degrade the electrical and mechanical properties of the FSS and supporting structures. Scientific instruments on spacecraft often have special additional requirements. If there are optics within the proximity of the FSS, there may be specific contamination requirements for material outgassing. A magnetometer scientific would also levy magnetic requirements within its field of view. This is just a brief list of environmental requirements that are general to most spacecraft. The specific mission and operation of the individual spacecraft will have direct requirements that must be incorporated into the design and fabrication of spacecraft FSSs.

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CHAPTER SEVEN

Active Beam Control Arrays

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With electronic devices embedded into their periodic cells, frequency selective surfaces (FSS) are capable of a broader range of functions. The earliest proposal for an array of this type appears to be that of Lee and Fong [1], involving the periodic loading of a corrugated surface with negative-resistance devices. It was envisioned that such an array would have the capability to amplify or shape a beam.

Aided by recent advances in the technology for high-frequency integrated circuits, such active FSS are now a reality. One simple form of active array consists of a metalization grid periodically loaded with biased linear diodes. Such an array is capable of modifying the amplitude or phase of a quasi-optical beam under external control. Since conventional high-frequency circuits that perform such functions are known as *control circuits*, this type of array has been given the name *beam control array*.

7.1 BACKGROUND

7.1.1 The Series-Resonant Beam Control Array

Beam control arrays developed up to now have been based on the series-resonant "self-resonant" grid [2, 3]. This FSS consists of an array of strips interrupted by gaps at periodic intervals (Figure 7.1a). In simple terms, this grid appears to a quasi-optical beam as an inductance (due to the strip array) in series with a capacitance (due to the gaps) (Figure 7.1(b)). In an active

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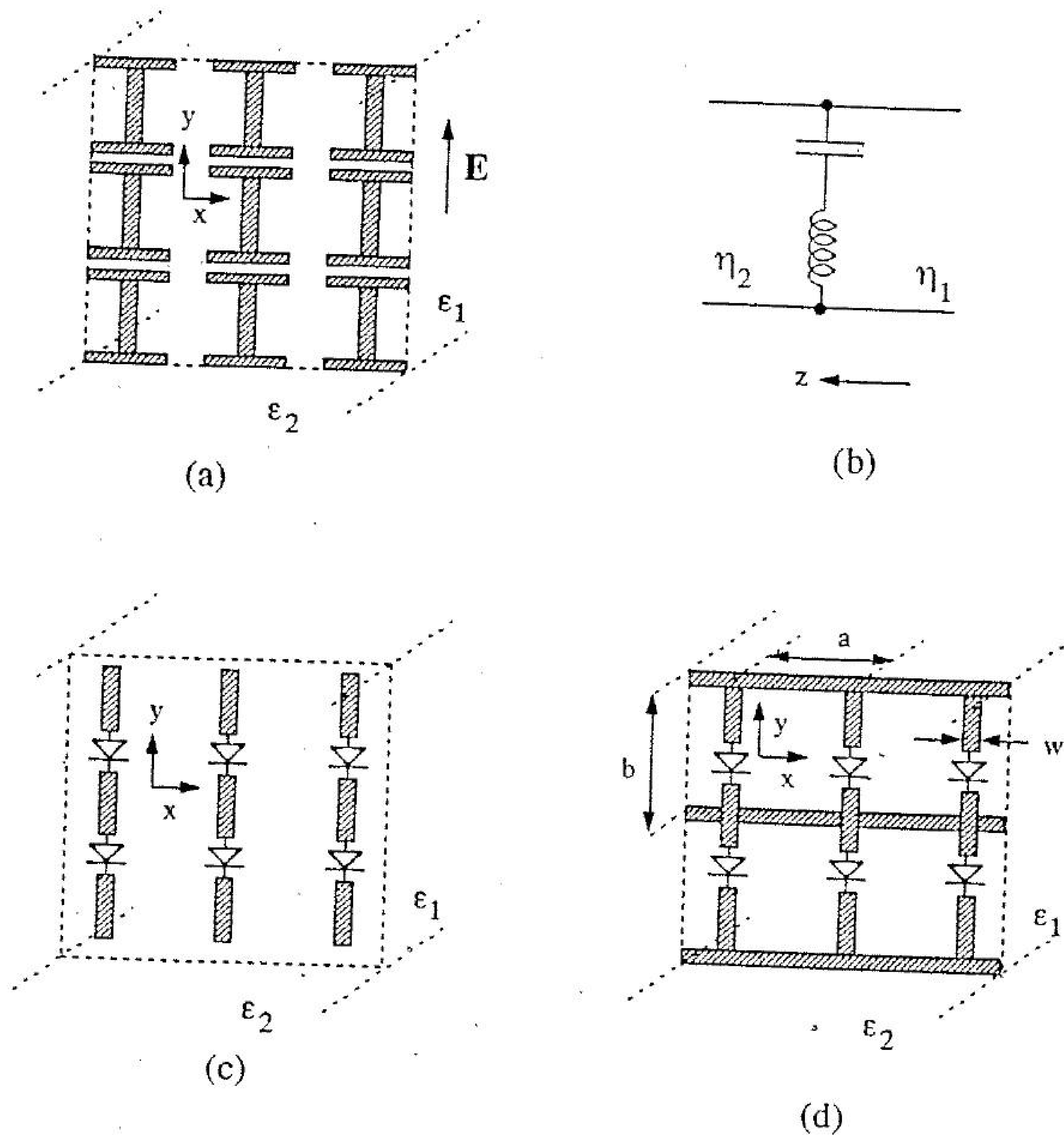


FIGURE 7.1 Origin of the beam control array. (a) Self-resonant series LC grid. (b) Equivalent circuit. (c) Active version of the self-resonant grid. (d) Same grid with the inclusion of the required bias lines. The x and y unit-cell dimensions are noted a and b, respectively, to match the notation employed for rectangular waveguide. The array operates on a beam with electric field polarized in the y ("active") axis.

array version, monolithically fabricated (e.g., varactor) diodes are placed across the gaps in the periodic structure (Figure 7.1(c)). The capacitance of the varactor diodes can be changed by adjusting the applied diode bias voltage, supplied by metal lines perpendicular to the diode embedding strips (Figure 7.1(d)). A change in varactor capacitance produces a change in grid impedance as seen by the quasi-optical beam, resulting in the beam control effect. The most practical modes of operation of the beam control array

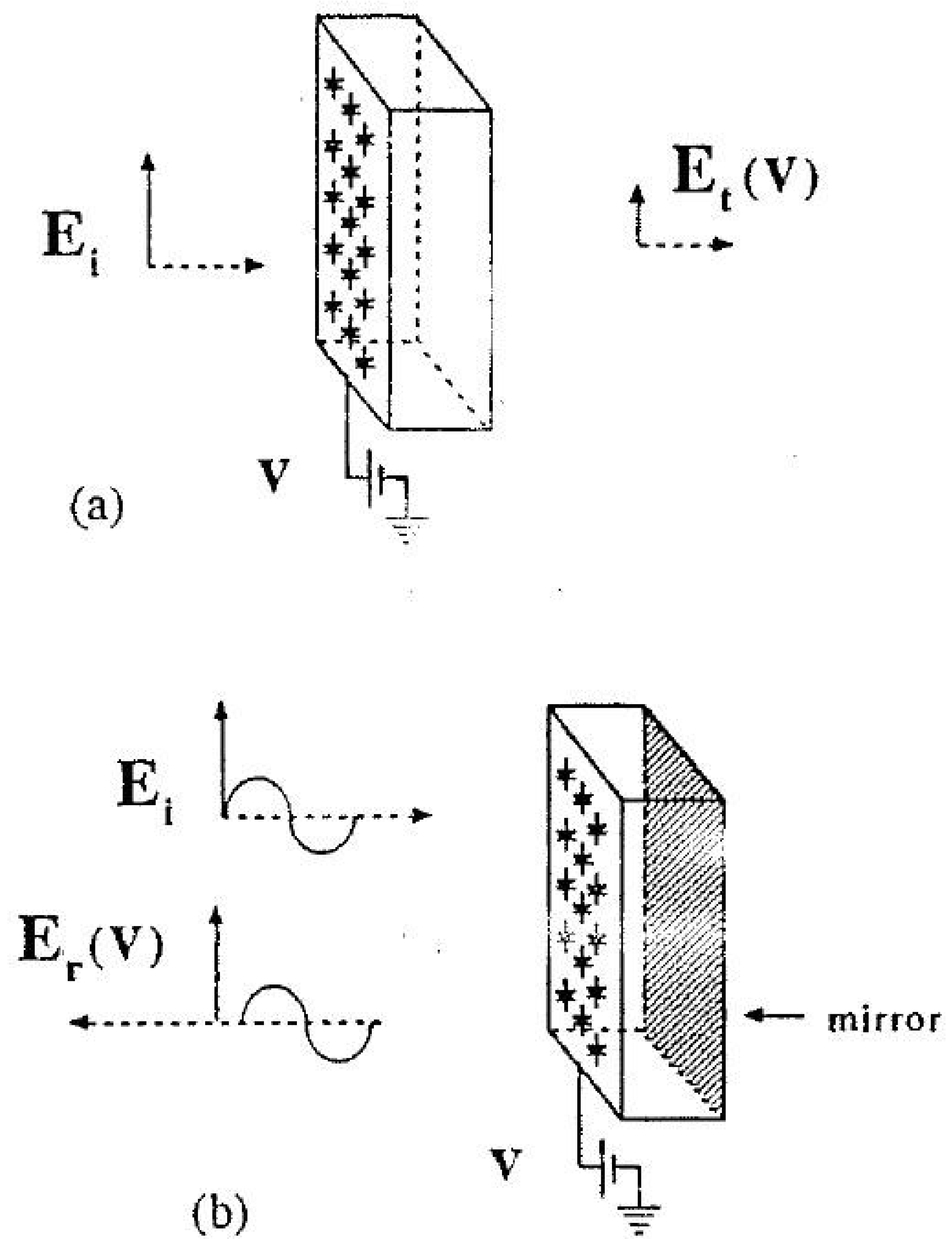


FIGURE 7.2 Modes of operation of the self-resonant LC grid. (a) Transmitted beam amplitude control. (b) Reflected beam phase control. (A mirror is placed behind the array for reflection operation.)

appear to be those of transmitted-beam amplitude control and reflected-beam phase control. These are illustrated in Figure 7.2(a) and 7.2(b), respectively.

7.1.2 Beam Control Functions

The first beam control function to be experimentally demonstrated was reflected-beam phase control. In this work [4], a phase range of 70°, with a loss of 6.5 dB, was achieved at 93 GHz. This was the first demonstration of a quasi-optical solid-state device array, and it led to the more recent demonstration by other researchers of multiplier arrays, oscillator arrays, and amplifier arrays.

It was postulated, in conjunction with the original phase-shifter array demonstration [5], that an array should be capable of beam steering and focusing if a nonuniform bias is applied to the array diodes. This has subsequently been experimentally verified [6], along with the more recently identified capability of beam polarization control [6].

TABLE 7.1. Demonstrated Beam Control Functions

Ref.	Function	Device	Cells	Freq (GHz)	Performance
4	Reflection phase shifting	Monolithic Schottky	1600	93	70°, −6.5 dB
9, 10	Transmission switching	Monolithic Schottky	4800	165	20–70%
11	Refl./Trans switching	Hybrid *p-i-n*	464	94	12.5–100% (refl.)
6	Reflection phase shifting	Monolithic Schottky	7168	120	60°, −3.5 dB
6	Reflection polarization	Monolithic Schottky	7168	120	0–.8 axial ratio
6	Reflection steering	Monolithic Schottky	7680	117	±5–7°
6	Reflection focusing	Monolithic Schottky	7680	120	Focus/defocus

Arrays that can vary the amplitude of a quasi-optical beam have also been demonstrated. In Langley and Parker [7], using an array of p-i-n diodes as a beam switch was proposed. Beam switching by a diode array was independently conceived by another research group, with the Schottky diode array "electronic shutter" proposed in King et al. [8]. In an experimental follow-up, such an array controlled the power transmittance of a 165-GHz beam between 20% and 70%, based on the applied voltage bias [9, 10]. The p-i-n diode array beam switch has now been demonstrated as well [11, 12]. Table 7.1 summarizes the quasi-optical functions demonstrated by beam control arrays.

The amplitude and phase control results in Table 7.1 apply at the single frequencies listed. In general, reflection phase control is limited to a small frequency range [6, Figures 6, 7], due to its reliance on the use of dielectric layers of thickness $\lambda/4$. Amplitude control [10, Figure 12] is possible over a wider bandwidth.

7.1.3 Practical Applications

A beam control array configured as a phase controller has several potential practical applications. Variable-reactance devices (varactors) are used as tuning elements in conventional electronic circuits. Similarly, a varactor-based beam control array can serve as a quasi-optical tuning element. In an experimental demonstration of this capability, a beam control array has been employed to provide voltage-controlled tuning of a quasi-optical oscillator array [13, 14]. Beam phase control also has potential application in communications systems. A suitably designed array should be capable of frequency-modulating a carrier beam, allowing information to be superimposed upon

the carrier. A grid array with phase control capability can also be employed to vary the polarization state of a quasi-optical beam [6]. An example application for polarization control [15] is reflected-beam switching.

Important additional practical applications exist for beam control arrays operated with nonuniform bias (phase). Biased for a linear progression of reflected-beam phase across its surface, a varactor array is capable of beam steering. The conventional planar phased array consists of a two-dimensional grid of active transmit/receive (T/R) cells. However, even with monolithic microwave integrated circuit (MMIC) techniques, such T/R cells are much larger than the $\lambda/2$ square dimensions required by such arrays if they are to perform large-angle scanning at millimeter-wave frequencies. Biased for a quadratic spatial phase progression from its center, a varactor array is capable of focusing a beam. This capability may be of interest for plasma diagnostic reflectometry [10], where a millimeter-wave probe beam is employed to determine the density profile of a plasma. Single-plane beam steering and focusing have been demonstrated by operation of the diode grid as a linear phased array. More sophisticated designs [16] should allow operation of diode arrays as two-dimensional phased arrays.

If phase control of a transmitted (versus reflected) beam is sought, a different design appraoch is necessary, since a series-resonant grid will block the beam in the low-impedance state. An array designed to be operated only far from resonance (at high impedance) will provide a low reflection coefficient, allowing the beam to be transmitted with low loss. Due to the limited reactance range, however, such a grid can only impart a small phase shift to the beam. To achieve a large (e.g., 360°) phase range, several grids must be stacked (this concept is motivated by analogous phase shifters designed in waveguide [17].) A quasi-optical design has been suggested for p-i-n diode grids [18], and developmental work has been performed on a similar design employing micromechanical switches [19]. For many applications phase control of a transmitted beam is more useful than phase control of a reflected beam; however, phase shifters based on this approach are likely to be quite expensive, due to the need for many stacked layers. A possible alternative has been suggested [15], based on the cross-polarization amplifier concept. The cross-polarization amplifier array [20, 21] employs transistors to amplify an incident beam polarized in one axis to a stronger beam polarized in the orthogonal axis. (Low-inductance) strip arrays are used as polarizers to separate the input and output beams. If varactors can be integrated into such arrays, simultaneous amplification and phase control may be possible [15].

Although beam amplitude control is a somewhat "simpler" operation than beam phase control, it is of considerable practical interest. By operation as a beam "switch" between the maximum and minimum achievable amplitudes, an array can be employed to pulse a radiating beam for pulsed radar applications. For radiometry, such an array can be employed as an electronic Dicke switch to chop an incoming beam, eliminating the need for the traditional mechanical rotating fan-blade chopper. The solid-state Dicke

switch offers attractive advantages such as the elimination of bulky and potentially failure-prone mechanical parts, as well as greatly increased switching speed for fast data acquisition, which is particularly important in imaging applications. As an analog device, the array has the capability of operating as a variable attenuator.

Additional amplitude control functions are possible if an array is operated with nonuniform bias. If the array, including biasing hardware, is designed to provide individual bias for each array element, then a locally addressed control should be possible in which only one pixel of the beam is transmitted or blocked [22]. In conjunction with a beam receiver, such an array should be capable of performing spatial imaging or near-field probing. A beam-switching array may also be employable to superimpose a spatial image onto a uniform beam. This would allow the transmission of an electronically programmable image through media opaque to optical frequencies. If a beam attenuator is operated under nonuniform bias, electronically controlled amplitude tapering of a beam should be possible.

Note that beam amplitude control will normally be accompanied by a phase shift. For pulsed radar applications, this should not present a problem. However, if an array is employed to create an amplitude taper in a quasi-optical phased array, the phase shift caused by the amplitude controller is an undesirable side effect. Although this might be compensable by adjusting the settings of the phase shifters, the preferred solution is to develop a more sophisticated amplitude control array design that minimizes the phase variation, just as MMIC attenuators are designed to minimize phase error.

One attractive feature of the beam control array is the potential for amplitude or phase control to be accomplished at high speed. The first evaluation of the speed capability of a beam control array was performed in Sjogren et al. [10]. The array exhibited a control speed of 100 MHz. Techniques for achieving higher control speed are discussed later.

7.2 THEORY

Beam control array analysis has been based on the quasi-optical approximation in which the beam is treated as a plane wave and the array is represented as an infinite two-dimensional grid of identical cells. A more sophisticated analytical treatment for active arrays has been presented [23], but the plane-wave approach has provided good results for the proof-of-principle experimentation performed to-date.

The array diode can be treated as a lumped impedance bridging an infinitesimal gap placed in the metallization strip. If the diode is short-circuited, the array is effectively an inductive-strip grid. The values of the array inductance can be estimated to reasonable precision with a quasi-static formula [24] or a variational formula [25]. Essentially the same solution results if the Green's function of the variational formula is employed in the

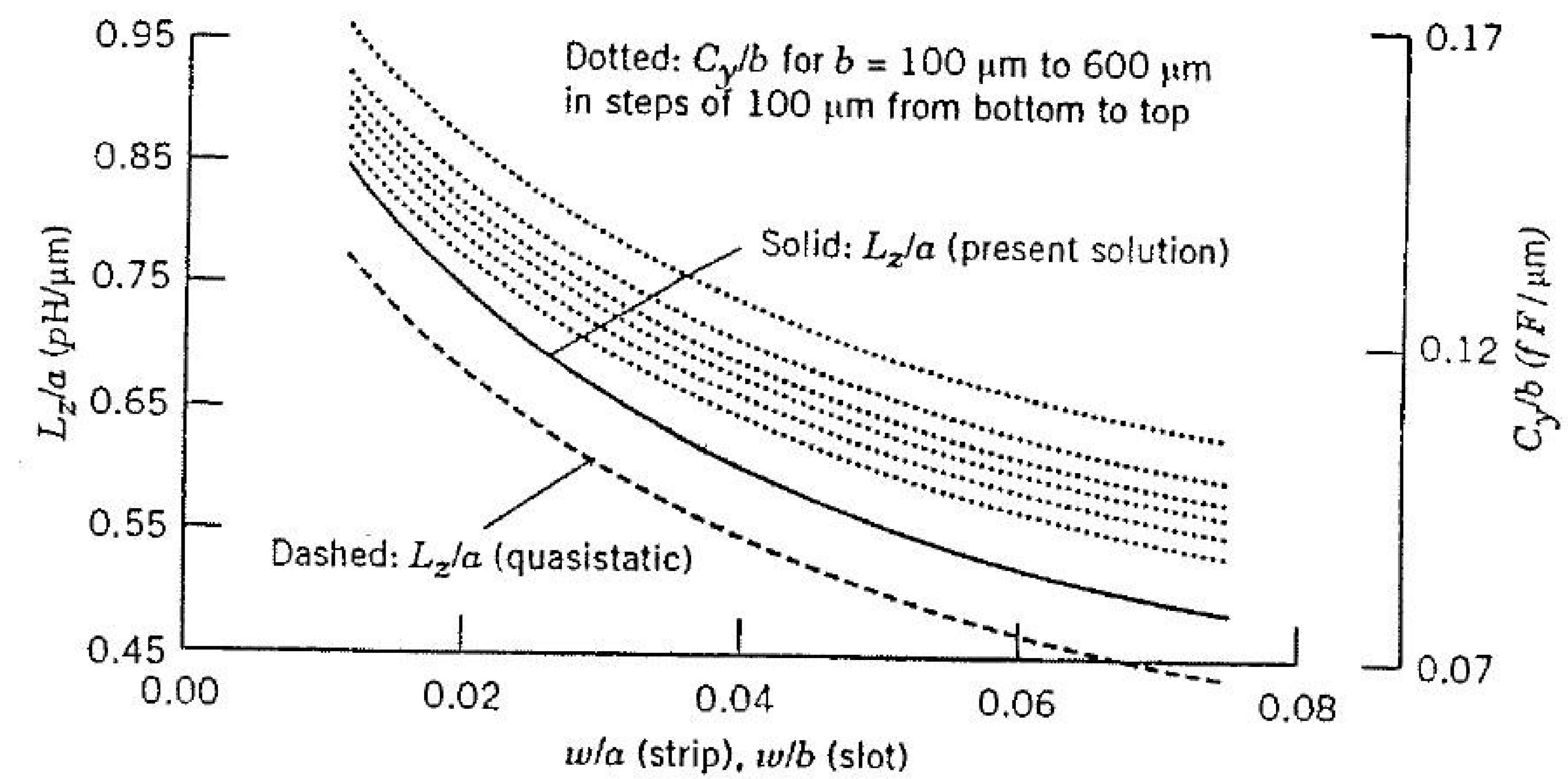


FIGURE 7.3 Inductance (L_z) curves for a strip grid array [26]. The curves are for 99 GHz, with an air to GaAs (ϵ_r = 12.9) interface. Also shown are curves for the capacitance (C_y) of the (dual) horizontal slot array. (©1991 IEEE.)

method of moments (MOM) with subdomain currents segmented along the longitudinal axis of the diode strip [26]. The solution, which gives equal amplitudes for the subdomain currents, is shown in Figure 7.3 along with the quasi-static solution.

If the diode is open-circuited, the array behavior changes. This condition can be simulated in the MOM solution by deleting one subdomain current element or by setting its self-element in the impedance matrix to a large value. This forces the current to zero at the diode site. The solution represents that of an inductive-strip grid whose strips are periodically interrupted by gaps. Not surprisingly, it is found that the array impedance in this case can be modeled as a series LC circuit. The capacitance of this circuit (called the grid capacitance) determined from the MOM is shown in Figure 7.4. The solutions of Figures 7.3 and 7.4 can be scaled to other frequencies by scaling all dimensions, inductances, and capacitances by f^{-1}.

Lumped impedances are treatable in the MOM by adding a term to the self-impedance element of the subdomain current whose local origin lies at the site of the lumped device. This allows the diode impedance to be included in the MOM analysis. The equivalent circuit model contains the diode impedance in parallel with the grid capacitance; this model provides a match to the MOM solution.

In addition to the grid inductance, grid capacitance, and diode impedance, some additional elements may warrant inclusion in the array impedance model. Figure 7.5 [10] provides a more complete model for the (varactor) diode array. The perpendicular metal strips (see Figure 7.1(d)) required for application of bias voltage form a capacitive (slot) array whose slots are

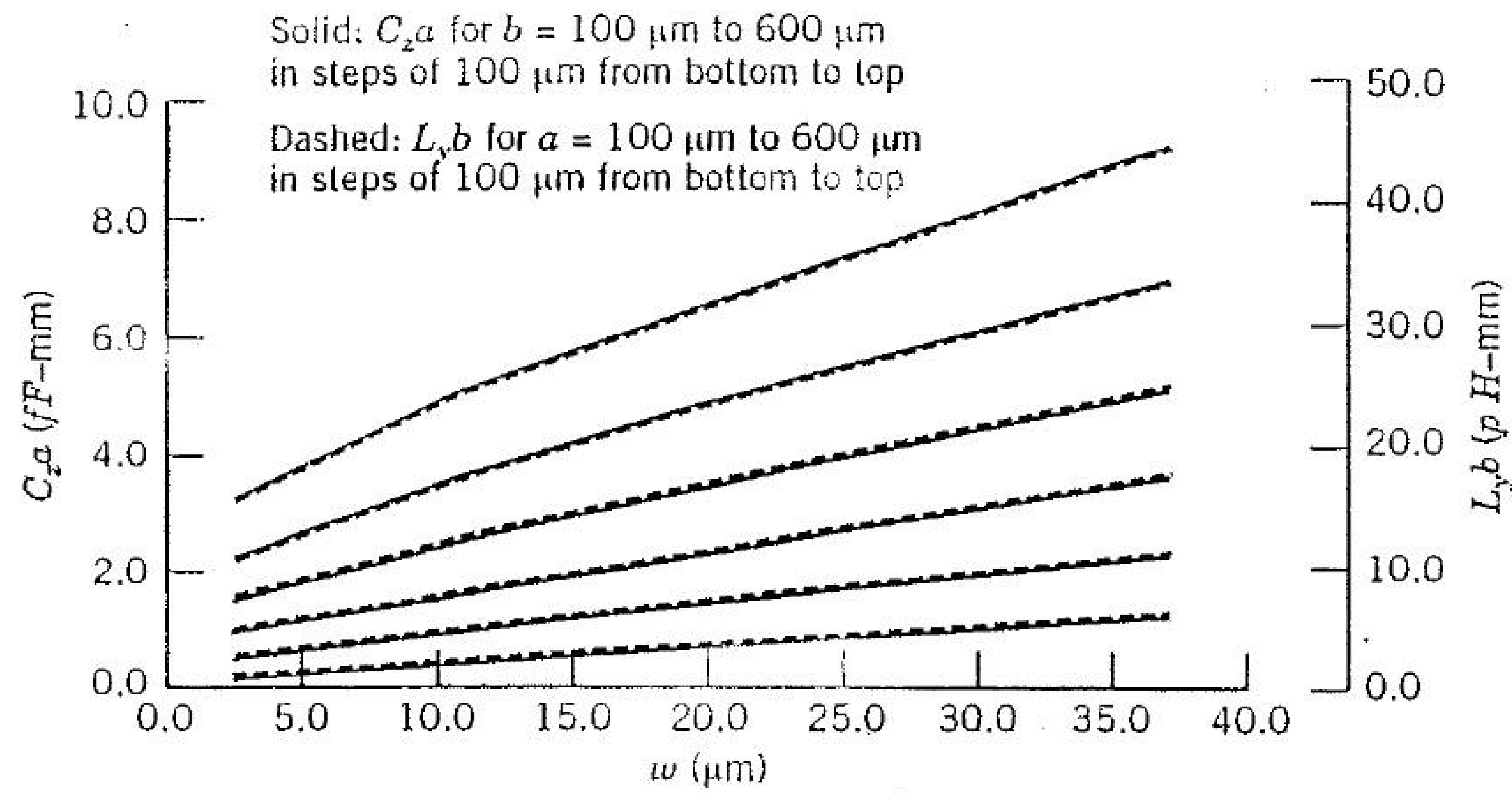


FIGURE 7.4 Grid capacitance (C_z) for a beam control array [26]. The curves are for 99 GHz, with an air to GaAs (ϵ_r = 12.9) interface. Also shown are curves for the inductance (L_y) (associated with the interruption of magnetic current by the embedded diodes) of the (dual) slot array problem. Note that the C_z and L_y curves are difficult to distinguish from each other because they are virtually identical and happen to overlap. (©1991 IEEE.)

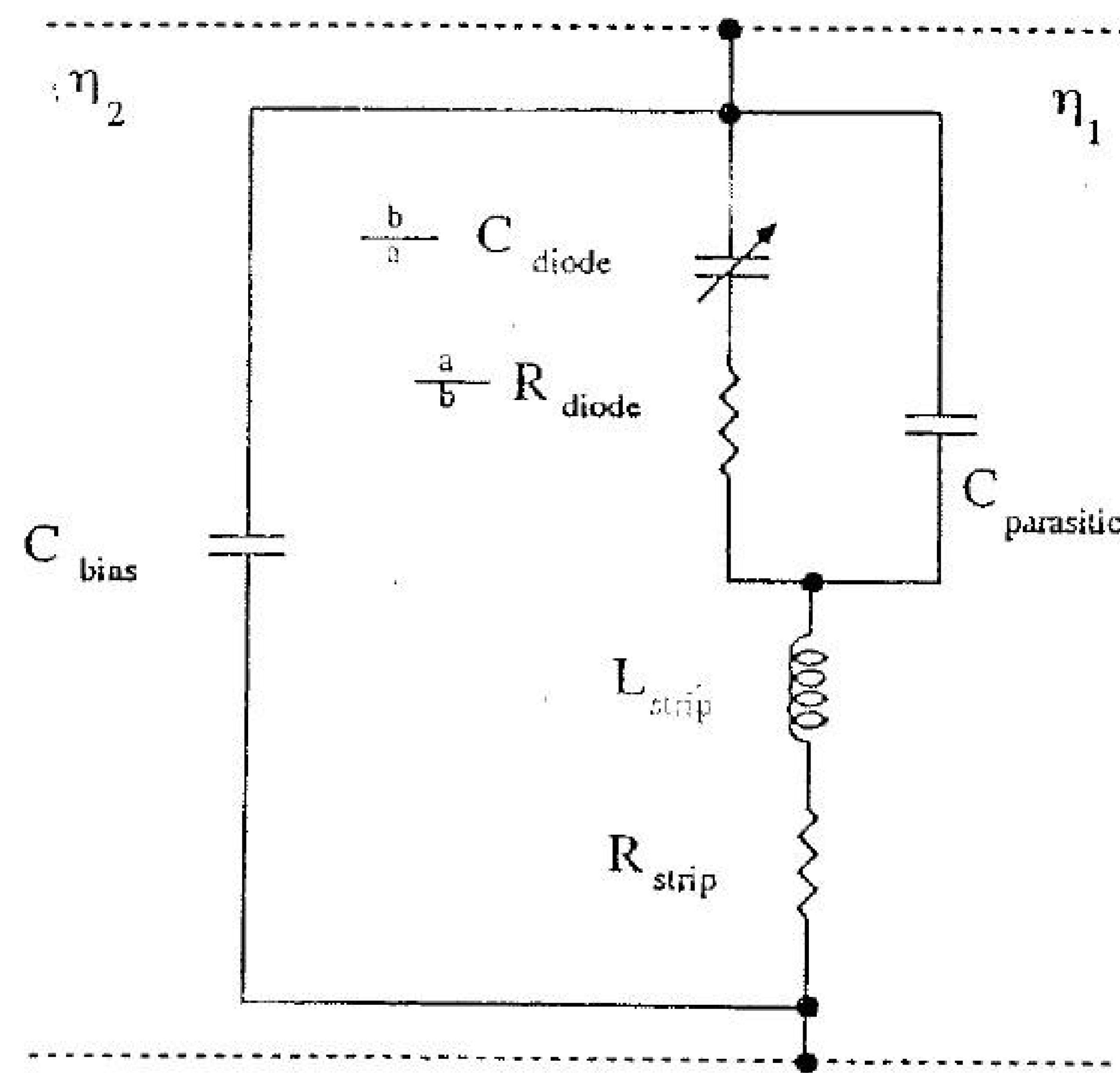


FIGURE 7.5 Circuit model for a (varactor) beam control array [10]. The array appears as a shunt impedance across transmission lines with characteristic impedance $Z_0 = \eta \equiv \sqrt{\mu/\epsilon}$. (©1993 IEEE.) Replacing the varactor diode resistor and capacitor with a single impedance $a/b\ Z_{\text{diode}}$ gives the general diode array model, where the "diode" may be the drain to source of a FET, a p-i-n diode, and so on.

extremely large. These are represented by the element C_{bias}. For the millimeter-wave arrays of Sjogren et al. [6, 10], the value of this element is approximately 2 fF. Due to its small magnitude and its presence outside the series-resonant circuit, this element has a minimal effect on the array behavior. The element R_{strip} represents the ohmic losses in the diode embedding strips.

7.2.1 Grid Capacitance

Note that the grid capacitance (Figure 7.4) is greatly reduced by closer spacing of diodes along the strip. Thus, a rectangular unit cell, with $b/a < 1$, can be employed to reduce the grid capacitance. Since this capacitance is roughly in parallel with the diode capacitance, it reduces the minimum achievable array capacitance and enhances the array capacitance ratio $C_r = C_{\max}/C_{\min}$, which largely determines the performance (amplitude or phase control) range of the (varactor) array.

The effective diode impedance scales with the aspect ratio, as indicated in Figure 7.5. This suggests that the effect of the rectangular unit cell, with $b/a < 1$, is to put a/b diodes "in series." The gaps that create the grid capacitance can similarly be interpreted as being "in series," although a decrease in b actually results in a stronger than b^{-1} reduction in grid capacitance.

If an array is designed with a reduced b dimension in order to suppress grid capacitance, the diode must be made larger to compensate for the change in effective diode impedance as a function of aspect ratio (Figure 7.5). This provides an additional benefit of the rectangular unit cell of an increase in signal power-handling capability by a factor $(a/b)^2$. The primary trade-off of this design is a slight increase in array resistance, since the resistance of a diode will not decrease linearly with increasing diode size, which would be necessary (Figure 7.5) for the quasi-optical resistance to remain unchanged.

In parallel with the grid capacitance will be a fixed parasitic capacitance associated with the geometry of the diode. In practice, these two capacitances are electromagnetically intertwined and can be lumped into a single element termed the parasitic capacitance, $C_{\text{parasitic}}$, as shown in Figure 7.5. An approximate estimate for the parasitic capacitance can be obtained by electromagnetic analysis of the true two-dimensional metallization pattern of the array unit cell, including the localized features in the vicinity of the diode. This was performed with a commercial simulation program [27] in Sjogren et al. [10]. Note that such a simulation will overstate the capacitance, since it ignores the fact that the diode will intercept some of the field lines, producing a "screening" effect. If a GaAs superstrate is present above the array, it has been suggested [10] that a simulation of the two-dimensional metal grid, with the substrate dielectric constant replaced by that of air to compensate for the screening effect, may provide a reasonable capacitance estimate. Note that with a superstrate present, it may be possible to reduce

the parasitic capacitance by etching cavities in the backside of the superstrate coincident with the diodes of the underlying substrate.

The grid capacitance may also be termed a "gap capacitance," since it is associated with the interruption of strip current at the diode sites. Its counterpart in microstrip is the capacitance of a gap in a continuous line. It is closely related to the capacitance of a gap in a mounting strip in rectangular waveguide [28], which can be represented as an equivalent problem involving a periodic array of currents. Alternatively, the quasi-optical array can be represented as a waveguide problem in which the unit cell is enclosed by electric walls on top and bottom and magnetic walls on the sides. Thus, the grid array and obstacle in waveguide problems differ only in the functional form of the waveguide modes (waveguide interpretation) or orientation of the image currents (infinite array interpretation).

7.2.2 Power Limitations

A major advantage of the quasi-optical device array is its ability to operate at high power levels by the spatial combining of the outputs from many devices. However, power handling is limited not only by the small-signal operation of the array devices but by heat dissipation as well. Since array unit-cell dimensions can be made quite small [9] (hence, device density can be made very high), heat dissipation will likely often be the limiting factor. A generic analysis of the heat dissipation properties of quasi-optical arrays is not possible because the thermal resistance depends on the mechanical configuration of the array and its mounting hardware.

Signal-level limited power-handling capability is, unlike heat dissipation, much more amenable to systematic evaluation. It is shown in Sjogren [16] that the power-handling capability of an array (with diode size adjusted to maintain the same impedance range) is proportional to b^{-2} with a constant a. The power-handling capability is unchanged for a change in a with constant b.

7.2.3 Other Considerations

All the analysis for beam control arrays performed thus far is predicated on the plane-wave approximation for the quasi-optical beam. In addition, the arrays are assumed to be of infinite extent in the transverse plane. Results indicate that these are excellent approximations for the arrays tested, whose transverse dimensions are 5–10 free-space wavelengths and that possess 30–100 elements in each transverse axis.

An additional assumption in the analysis has been that of normal-incidence and uniform-bias operation. Some of the experiments (cited in Table 7.1) have deviated from these conditions, but only slightly. With a small variation of the reflection phase across the array, it is reasonable to assume that the phase at a local region with a given applied bias is the same as that

for uniform array operation at the same bias. When large-angle beam steering is attempted, this approximation will no longer be valid. More rigorous analytical treatment will be highly advantageous in the development of arrays capable of highly nonuniform operation.

The presence of faulty and nonuniform array cells obviously will also affect array behavior. Strictly speaking, the "error currents" in the vicinity of a defective cell (those, which when added to those associated with a perfect array, sum to the actual current distribution) will radiate a continuous spectrum of spatial frequency components, and the plane-wave representation becomes invalid. For practical arrays, which possess a small percentage of defective cells, the performance still conforms to the plane-wave model, but the model parameters must be adjusted to account for the nonidealities. (This is discussed further later.) Analytical investigation of the effect of array defects is probably unwarranted, since the incidence of cell defects can be expected to decrease as the technology is further developed.

More recent beam control array work has assumed the substrate is lossless. The beam power in a dielectric substrate is $P = P_0 e^{-2\alpha z}$, where $\alpha = \sqrt{\omega\mu_0\sigma/2}$ is the field decay per unit distance due to dielectric loss, and z is the depth of the beam into the substrate from the surface ($z = 0$) of incidence. Assuming microwave-grade GaAs material with a bulk resistivity around 1×10^8 Ω-cm [29], with a 100-GHz beam, the power is $P = P(0)e^{-4.0z}$ (z in meters). Thus, the power loss for a beam to traverse a typical array (e.g., 0.002 m thick) is small, even accounting for the fact that the beam power, on average, may traverse the array several times due to internal reflection. This also holds for typical dielectric materials within which the array may be stacked (e.g., SiO_2, Al_2O_3, BeO, or AlN). However, it may not apply for an array fabricated on silicon, which has a much higher dielectric loss.

7.3 DESIGN

7.3.1 Device Design

Semiconductor devices suitable for application in traditional high-frequency (e.g., guided-wave-based) control applications are the logical candidates for application in beam control arrays. One major difference in the choice of the optimal device, however, is that the power-handling capability of the individual device is much less important in quasi-optics. This is due to the ability to power-combine spatially the outputs of thousands of devices in a single quasi-optical array.

The array device employed must obviously be suited to the function that the array is intended to perform. For variable-phase control, varactors are required. For variable-amplitude control, p-i-n diode or field-effect transistor (FET) varistors may be used. However, as shown by Sjogren et al. [9, 10],

varactor diodes can also be employed for this function. If a digital [30] array design (one in which the impedance is switched between two or more discrete states) is used, the appropriate array device is one that can perform as an effective solid-state switch. The p-i-n diode, Schottky varactor, and FET can all be employed as a radio-frequency (RF) switch.

In general, III-V (e.g., GaAs) material-based devices are desirable because of their high speed and low substrate loss. Schottky varactor diodes have been employed in the majority of beam control arrays demonstrated so far because of their analog control capability, extremely high frequency capability, negligible dc power consumption, and relatively simple fabrication. P-i-n varistor diodes provide a large "on-state" to "off-state" impedance ratio, which is useful for switching applications. In addition, they possess a high RF power-handling capability. On the other hand, the forward bias current (on the order of milliamps) requirement for the p-i-n diode results in the generation of a substantial amount of heat, and the switching speed of a p-i-n diode is less than that of a Schottky diode.

A potential alternative to the p-i-n diode for switching applications is the III-V FET (e.g., metal-enhanced semiconductor FET (MESFET) or high-electron-mobility transistor (HEMT)). The FET can be operated as a control device with negligible dc power dissipation. Although FETs are more complicated to fabricate, they are the most commonly used high-frequency devices, and custom monolithic FET circuits can be purchased from III-V semiconductor "foundry" operations. The FET is the device with the most apparent usefulness for beam control that has not yet been tried. For low-cost operation in the lower end of the microwave region, the Si-based metal-oxide semiconductor FET (MOSFET) may be of interest as a substitute for the III-V FET. However, the bulk resistivity of silicon substrates employed for standard MOS integrated circuits is sufficiently low that arrays employing them will suffer very large dielectric losses. Higher-resistivity wafers are available, however. The technology of silicon on insulator (SOI) may solve the problem of substrate loss, but it probably has not yet reached the level of maturity that would warrant its application to beam control arrays.

Diodes fabricated on III-V epitaxial wafers have been employed in beam control arrays. Figure 7.6 illustrates an epitaxial wafer profile for the fabrication of Schottky varactor diodes. When a small-signal voltage is applied to the diode, an equal and opposite charge appears at the (metal) Schottky contact and at the "depletion region boundary," which lies in the n-doped epitaxial layer. Thus, the diode behaves as a parallel-plate capacitor whose "plates" are represented by the Schottky contact and depletion boundary. A change in the applied bias voltage across the diode shifts the position of the depletion boundary, which changes the separation of the "plates" of the capacitor, resulting in the voltage-variable-capacitance characteristic.

One device design issue is the choice of doping profile. There is no single "ideal" doping profile. In general, it is desirable to achieve a large capacitance ratio between the maximum and minimum bias states with a doping

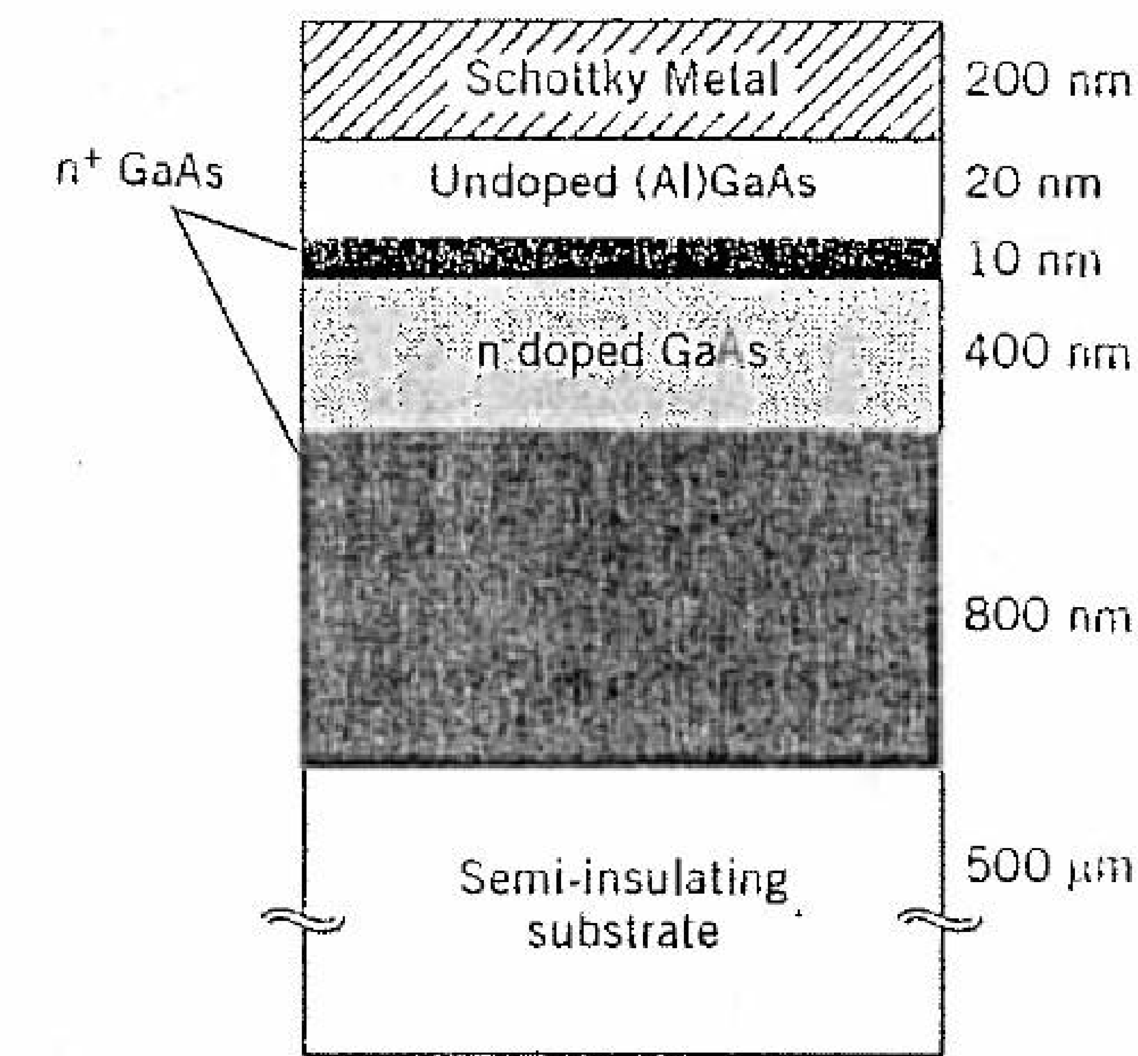


FIGURE 7.6 Epitaxial structure for a III-V varactor beam control diode.

profile that allows the depletion boundary to be shifted over the widest possible range. Placement of a high-doped (1–2×10^{18} cm^{-3}) layer near the Schottky contact assists in achieving a large maximum capacitance, C_{max}, by allowing the depletion region boundary to be pushed close to the Schottky contact at forward bias, with a sufficient potential barrier remaining so that conduction current is acceptably low. It is not clear, however, that doping right at the Schottky contact is advantageous, since the depletion charge associated with such doping translates to only a small potential upon double integration of the charge over the small distance from the Schottky contact. Recent beam control arrays have employed a high-doped region (0.5–2×10^{18} cm^{-3}) between 200 Å and 300–400 Å from the Schottky contact. Beyond this depth, a much lower doping is desirable, since continuous high doping will reduce the breakdown voltage, limiting the maximum depletion region depth and, consequently, the achievable minimum capacitance, C_{min}. The doping should not be made too low, however, since that may lead to an undesirably steep variation of capacitance versus voltage and will increase the resistance of the diode when the depletion region boundary is shallow (in the more positive voltage portion of the diode bias range). One characteristic of an optimized design is that breakdown occurs just as the depletion boundary reaches the bottom of the n-doped region. Undepletable n material simply adds resistance without increasing the capacitance range. If the depletion boundary reaches the n^+ region prior to breakdown, on the other hand, then some of the breakdown voltage has been "wasted," since the depletion region boundary will go negligibly deeper once it has reached the n^+ region.

The C-V characteristics for a Schottky varactor diode can be estimated by a one-dimensional solution to Poisson's equation [16]. However, this solution

does not include parasitic fringing capacitance, which will increase C_{min}. In addition, diodes with a predicted C_{max} based on a depletion depth of 300 Å show an actual C_{max} corresponding to a depletion depth of 500 Å. These values were obtained for large-area test devices, so the variance from theory is not due to fringing effects. For the small diodes necessary for high-frequency beam control, fringing capacitance is also present. A diode designed with an n region from 300 Å to 4000 Å could theoretically give a capacitance ratio C_{max}/C_{min} of 13 : 1. In practice, a well-fabricated diode may exhibit a ratio of 5 : 1, and the quasi-optical behavior of the array may exhibit an effective ratio of only 3 : 1.

In addition to doping profile, the material composition must be chosen for the epitaxial III-V diode. The first beam control array [4] employed pure GaAs, and the second (denoted PS1) [9] employed a surface layer of (wider band gap) AlGaAs, which was previously proposed for frequency-multiplier diodes [31]. AlGaAs possesses a lower dielectric constant than GaAs, which reduces C_{max} at a given depletion depth. However, an AlGaAs layer should allow a larger (forward and reverse) bias to be applied due to the suppression of conduction current. Although it is likely the net effect of the AlGaAs layer is beneficial, to the knowledge of this author, there has not been a conclusive experimental confirmation of this.

A promising alternative material structure is the superlattice barrier [32]. Here, a set of alternating thin layers of narrow-gap and wide-gap material is used instead of a single wide-gap layer. Another promising new approach involves use of a (non-lattice-matched) single-barrier layer of material possessing a high Schottky barrier energy [33]. Varactor diodes may prove more tolerant than FETs of crystal lattice mismatch.

7.3.2 Monolithic Device Configurations

Several advances have been made in beam control array designs since the original work of Lam et al. [4]. That design consisted of an array of 1600 identical square diode cells (Figure 7.7a) repeated in the x and y axes.

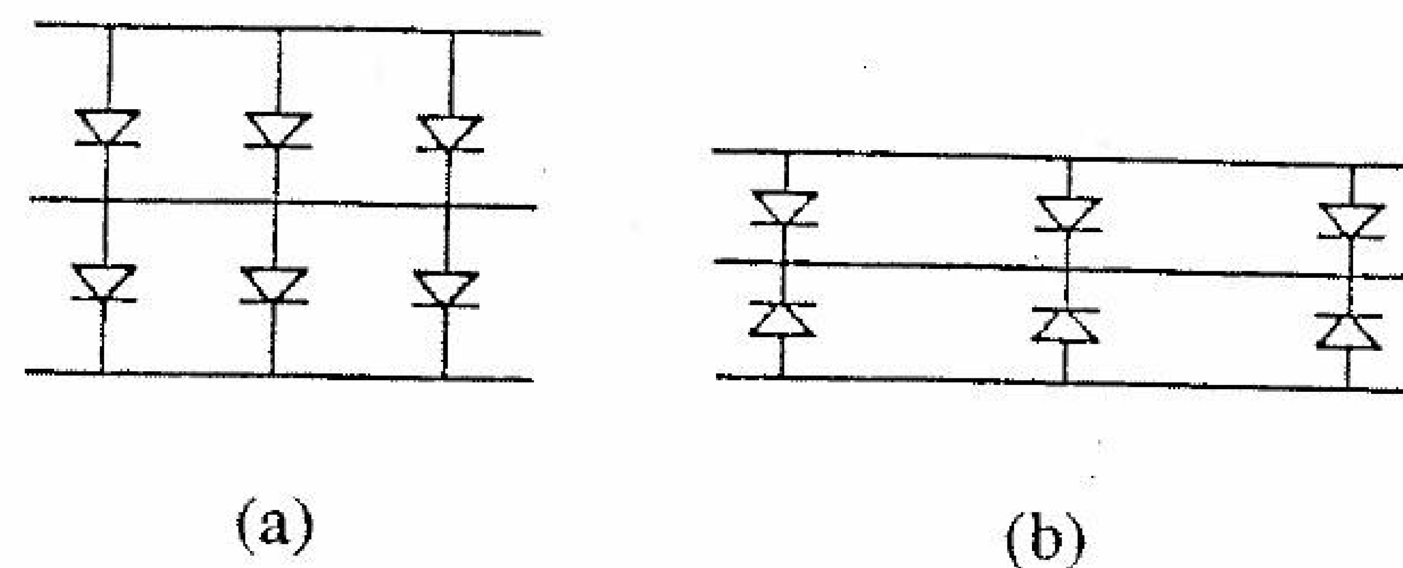


FIGURE 7.7 (a) Single-ended diode in square unit cell. (b) Single-ended diode in rectangular unit cell.

The second beam control array design (PS1) is shown in Figure 7.7(b). This design employed two new features–rowwise alternation of diode orientation and a rectangular unit cell. Diode alternation allows the use of single-ended dc supplies for biasing. The rectangular unit-cell design reduces parasitic capacitance, as discussed earlier. A microscope photograph of a fabricated array of this design is shown in Figure 7.8.

The antiseries biased diode (ABD) [22] represents another promising design technique. The ABD is an extension of a design conceived for frequency-multiplier varactors, in which a pair of diodes is monolithically integrated in a back-to-back (antiseries) configuration [31]. For discrete devices there is no advantage to such an arrangement, but for monolithically integrated diodes it is beneficial, because the ohmic (cathode) contact is eliminated from the RF path. The ohmic contact is a major contributor to the resistance of a single-ended diode; hence, the back-to-back design substantially reduces the RF resistance. This advantage is partially offset, however, by the fact that the ratio of maximum capacitance to minimum capacitance of the diode pair is reduced from that of an individual diode, since an applied (RF) signal tends to forward bias one of the diodes as it reverse biases the other in the antiseries pair.

In the ABD a third terminal is applied between the back-to-back devices, which allows them to be simultaneously biased to the desired low- or

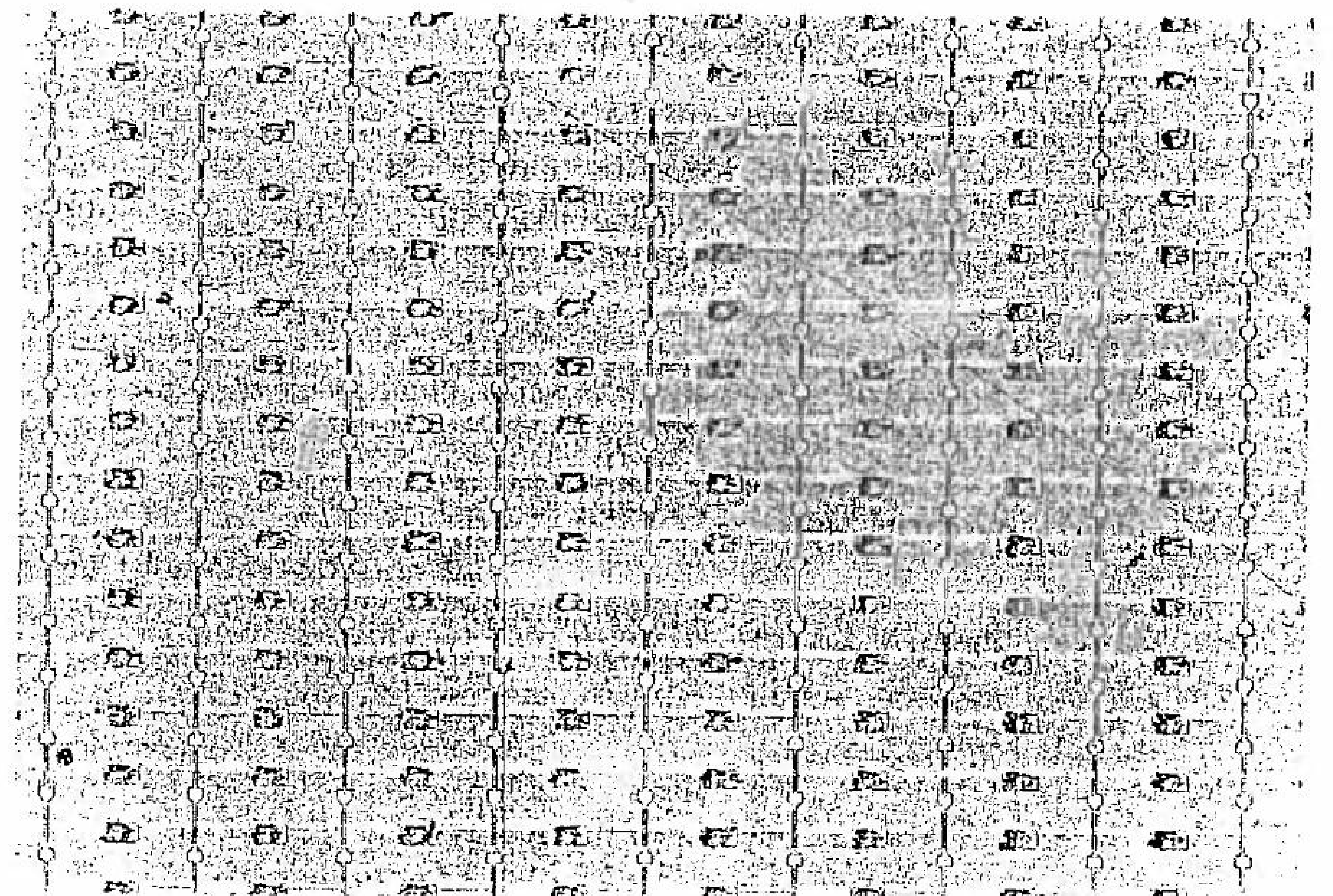
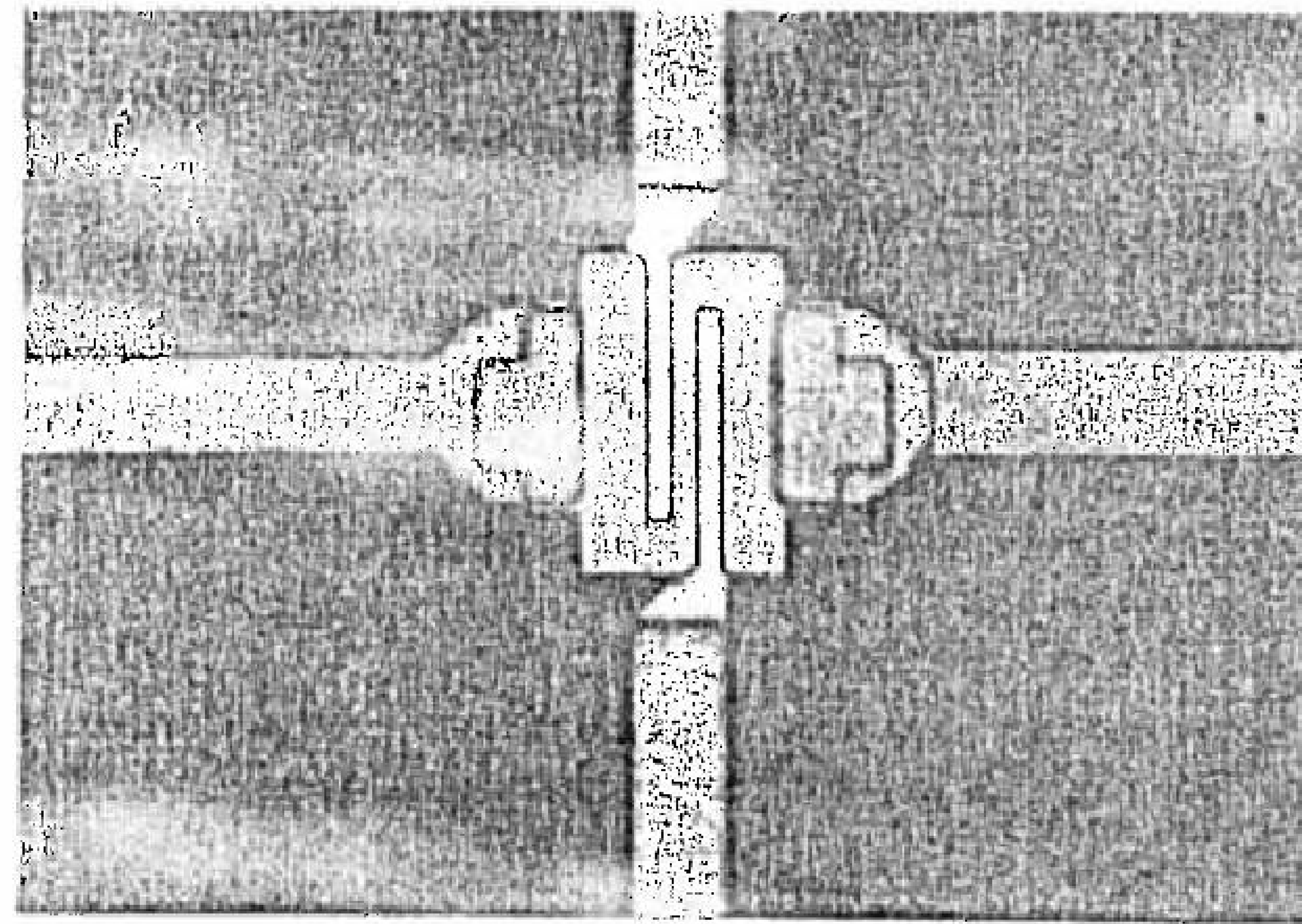
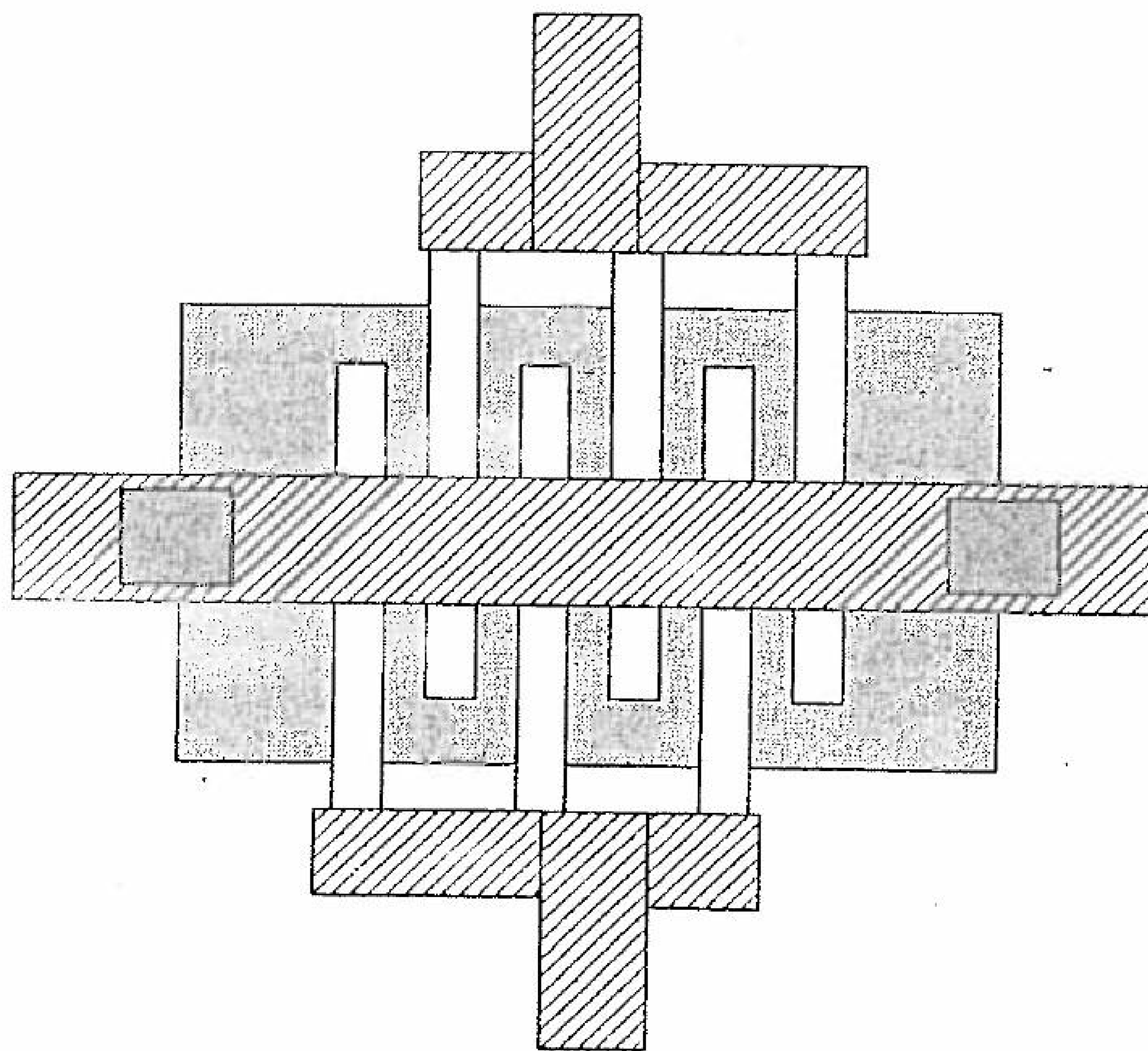


FIGURE 7.8 Microscope photograph of a (single-ended diode) PS1 array.



(a)



(b)

FIGURE 7.9 (a) Microscope photograph of an ABD device. (b) Proposed higher-performance ABD.

high-capacitance state. The ABD, in conjunction with the rectangular unit-cell design, provides the potential to achieve low array resistance and low minimum capacitance. An ABD array (denoted PS2) has been successfully constructed and operated as a quasi-optical phase shifter [6]. A fabrication problem (substantial etching of the anode contacts) resulted in a much higher than expected resistance. Although the low resistance of the ABD has yet to be experimentally demonstrated, there is little doubt that it can be achieved, since it is predicated simply on Ohm's law calculations. A device from the PS2 array is shown in Figure 7.9(a), with a more advanced concept [22] for an ABD in Figure 7.9(b). Here, an ohmic contact is not fabricated between the Schottky leads. This permits the Schottky metallization to be fabricated by the liftoff process, and the leads can be spaced at the minimum linewidth for the process, which may be a fraction of 1 μm, reducing the lateral RF resistance of the back-to-back structure. To pass the cathode bias along the diode row efficiently, one should use a second-level metallization, as shown. The strip "above the diodes" adds some capacitance, but it should not be a major concern if the metal is fabricated on top of a dielectric (e.g., nitride) separation layer with sufficient thickness.

The ABD design involves two devices that appear in series to the RF but in parallel to the dc. A monolithic design employing a similar idea for gain devices also appears to be feasible. The "FET negistor" has been conceived as a means to accomplish this [15]. This design has interesting possibilities for application to beam amplification and may provide a basis for lossless beam control by the use of varactors and negative-resistance devices in the same array [15].

The ABD is not applicable to circuits requiring a device with asymmetric C-V or I-V characteristics. For such applications, the surface channel varactor [34] is typically employed. It should be considered a viable candidate, along with the ABD, for beam control array applications. Conversely, the ABD may warrant consideration for some applications (e.g., subharmonic mixers) [35] in which surface channel varactors are used.

7.3.3 Grid Design

The series-resonant strip grid has been employed for beam control arrays to date. However, other grid designs are possible. A horizontal slot array is the electromagnetic dual of a vertical-strip array. A diode-embedded slot array can be modeled [26] similarly to the strip diode array. An additional impedance element can be introduced in the strip and slot arrays by truncation. The values of these additional elements can be evaluated by a MOM analysis [26], but with a group of the subdomain elements removed. Figures 7.10(a) and 7.10(b) show the truncated strip and slot arrays, respectively. Similar behavior to the truncated strip array should be exhibited by the

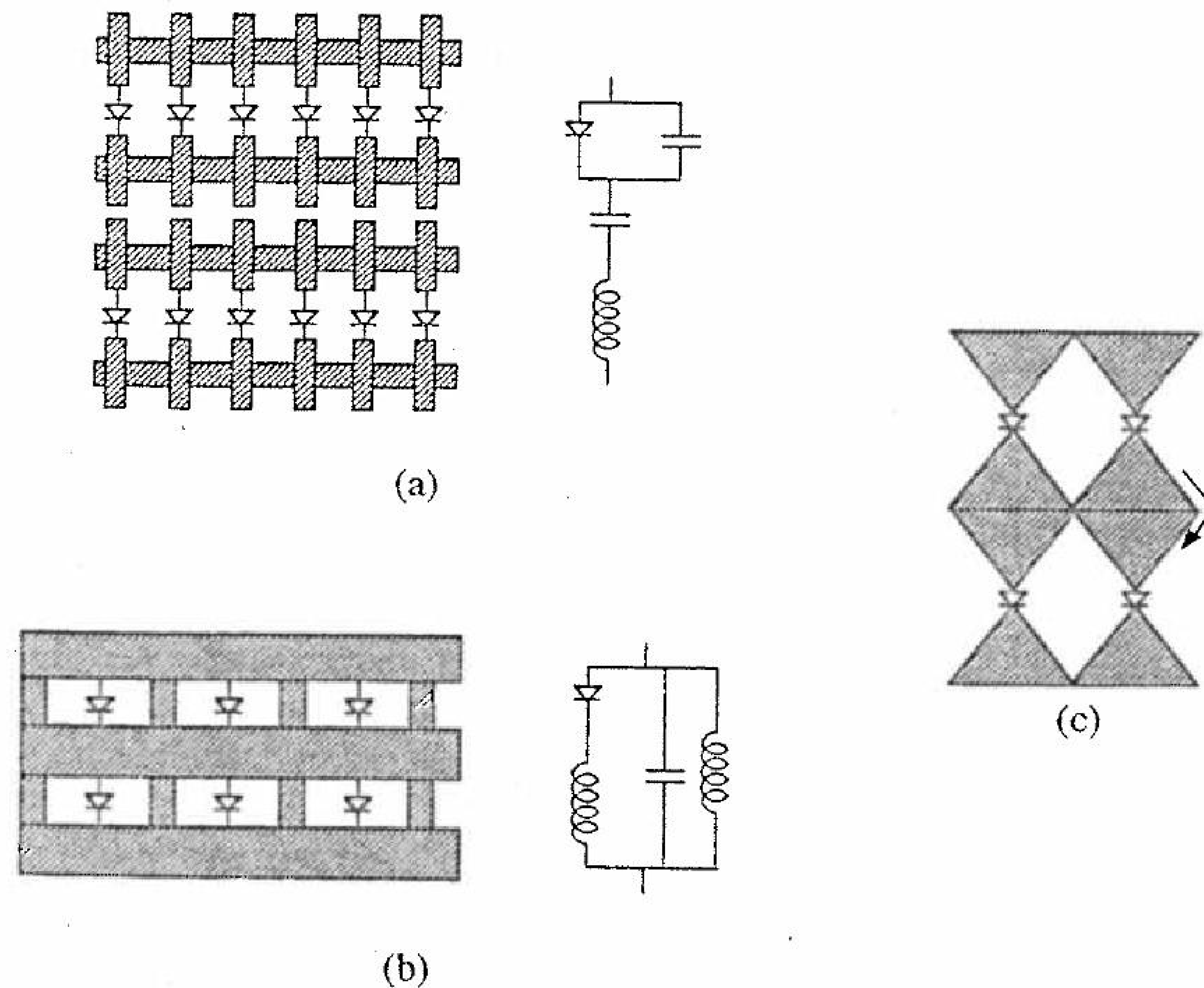


FIGURE 7.10 Some grid options for beam control arrays: (a) truncated strip array, (b) truncated slot array, (c) bow tie.

square-loop array [36]. As shown in Figure 7.10(b), the truncated slot array will shortcircuit the diodes, but integration of blocking capacitors would allow construction of a biasable truncated slot array.

The bow-tie antenna [37] can be considered a generalization of the strip and slot antennas. To the knowledge of this author, an analytical treatment of the bow-tie in array form has not yet been published. One potential approach would be to perform a MOM analysis using "bent" piecewise sinusoidal dipoles, such as have been successfully employed in a spectral-domain analysis of microstrip "wire" antennas of various shapes [38]. The bent dipole provides an appropriate representation of the current shown in Figure 7.10(c). This subdomain function, however, has the undesirable property of an infinite spectrum of nonzero spatial frequency components for the x axis, because of the change of the direction of the current (even though Kirchhoff's current law is satisfied). The solution for a single-microstrip antenna is possible because an asymptotic solution can be extracted from the spectral-domain integral. In contrast, an asymptotic solution for the infinite periodic array is not available.

The simple (nontruncated) inductive-strip array is a good match with a variable-capacitance device, since the design allows the array impedance range to be centered at zero reactance, which maximizes the phase range of the array [15]. Variable-capacitance diodes could also be embedded in a slot array, although the phase range will be reduced.

A recent publication [39] has proposed configurations in which FETs can operate as "active" (voltage-controlled) inductors. If such a circuit can be employed in place of a variable-capacitance diode, a slot array could then be constructed as a parallel-resonant LC circuit. The performance range of such an array should be similar to that of the series-resonant grid. However, it is not clear whether an active inductor circuit can be devised that is sufficiently compact to be used as the active element in a quasi-optical array. In addition, biasing may be a challenge, and operation will be limited to the lower frequencies at which FETs can perform efficiently. The use of a passive grid in conjunction with a slot array provides another means of constructing a parallel-resonant quasi-optical circuit. An inductive grid separated by $\lambda/2$ from the slot array, or a capacitive grid separated by $\lambda/4$, will create such a circuit.

7.3.4 Quasi-Optical Circuit Design

The beam control array can be considered a single component of a quasi-optical circuit, which may contain more than one grid array [13, 14] and additional dielectric slabs and/or passive FSS. The ability to model such circuits with a transmission line representation allows circuit analysis to be performed similarly to that employed for microstrip or waveguide circuits.

A quasi-optical circuit employing a single grid array may provide enhanced performance by the inclusion of plain dielectric slabs. Fused silica ($\epsilon_r = 3.83$) is useful in conjunction with semiconductor substrates, which typically have a relative dielectric constant of 10–15 (ϵ_r for GaAs is 12.9). With a dielectric constant between that of air and the semiconductor substrate, a fused-silica slab can provide a (smoother) two-step impedance transition. In general terms, the presence of such slabs serves to reduce the reflections at the air-to-semiconductor surface, resulting in quasi-optical behavior dominated by the variable-impedance grid rather than reflections at dielectric interfaces. Employed as a cover layer of a reflection phase shifter, such a layer will increase the phase range (at the expense of some loss). Employed on the input and output side of a beam transmission controller, such layers improve bandwidth and may help obtain a stronger beam in the transmitting state.

A greater performance range can be achieved by (reflected-beam) phase-shifter arrays if two are stacked [5]. In principle, 360° of phase range can be achieved by a two-grid stack, although in practice this may prove difficult. One reason for this is that, when an array is stacked under another array, the high dielectric constant for the medium above the array plane will increase the parasitic capacitance of the array. If necessary, more than two grids can

be stacked to increase the phase range [6]. With three stacked grids, 360° of phase range should be possible to achieve with a modest value of C_{max}/C_{min}. Beam power losses, however, will tend to increase as more arrays are stacked. Consequently, such arrays will perform best if they incorporate low-resistance (e.g., InGaAs) devices or active devices providing negative resistance that cancel the losses [15].

7.3.5 Thermal / Mechanical Design

Of all the design aspects of beam control (and other active) arrays, the mechanical design is the least developed. Proof-of-principle experiments have been performed with arrays mounted on a printed circuit board that provides the array bias or control signals through wire bonds. Figure 7.11 shows an assembled (PS1 or PS2) array. Beam control arrays employed for practical applications will require much more sophisticated mechanical designs.

Although quasi-optical arrays offer high operating power by the large-scale integration of devices, such power implies a commensurate large amount of heat to dissipate (except for the Schottky varactor or FET switch array). As for conventional MMICs, the heatsinking problem is most severe in the vicinity of the device, since the heat is generated in a very small region. This can be illustrated by an approximate analysis of the heat flow from the device to backside of the substrate. Figure 7.12 illustrates the geometry. The heat

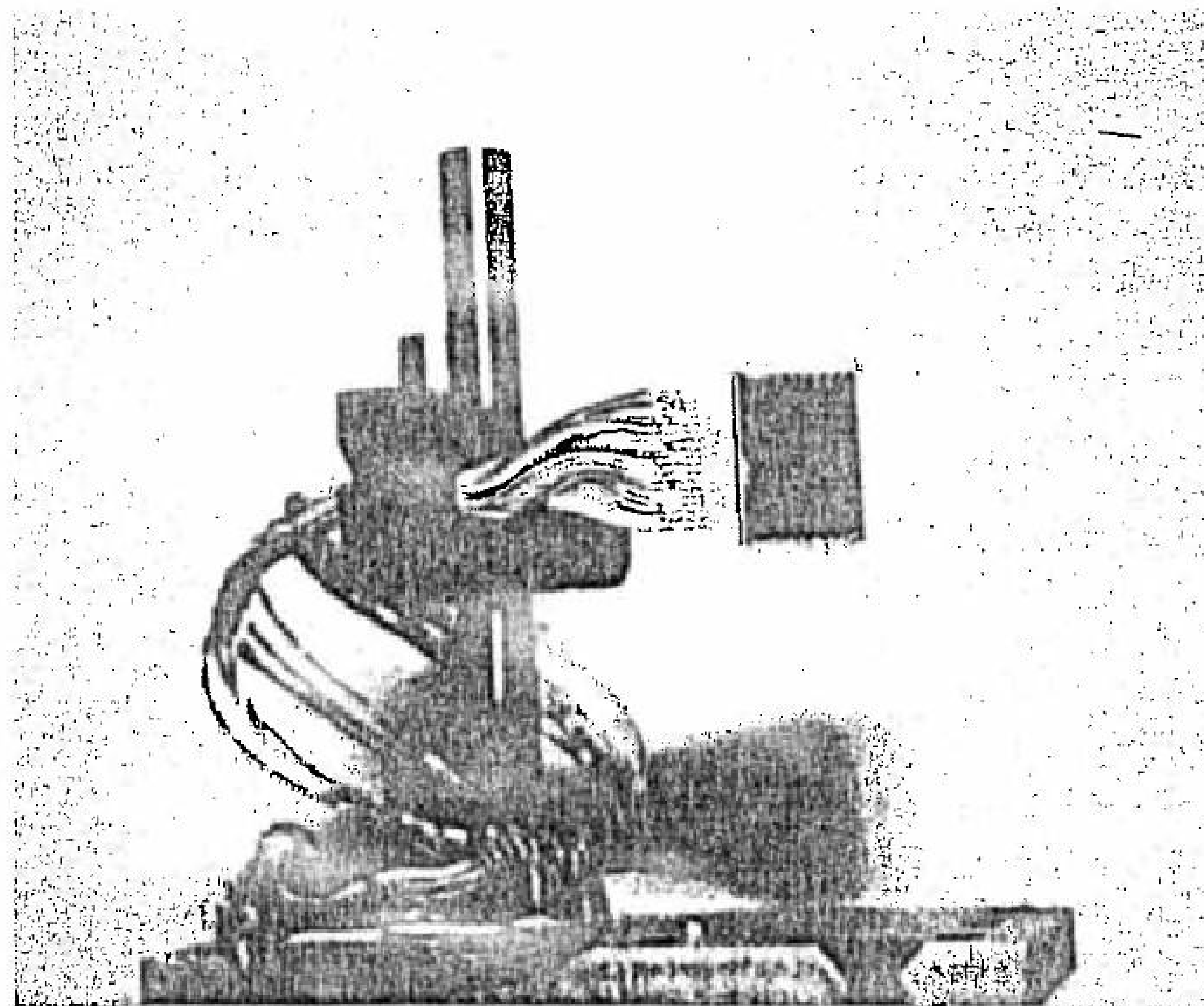


FIGURE 7.11 Assembled beam control array.

from a (round) diode is assumed to emanate from a circular region in the device plane of radius r_0. We assume that the cross-sectional area of heat flow is a circle diverging from the source with an angle of 45°. The thermal resistance (temperature difference divided by dissipated power) is

$$R_{th} = \frac{\Delta T}{P} = \int_0^t \frac{1}{A(y)\sigma_{th}}\,dy,$$

where $A(y)$ is the cross-sectional area at depth y, and σ_{th} is the thermal conductivity of the substrate. For the current example, this integrates to

$$R_{th1} = \left\{\frac{1}{r_0} - \frac{1}{r_0 + t}\right\}(\pi\sigma_{th})^{-1}.$$

With, for example, a 5-μm diode, on even a very thin substrate of 100 μm, the substrate thickness has negligible effect. For a much thicker array, however, a depth will be reached at which the heat from one device meets that from the devices in the adjacent array cells, and heat spreading no longer occurs. The "cones" from the array devices will overlap roughly when the substrate thickness equals the array unit-cell dimensions. Beyond this depth the temperature distribution may be approximated as uniform, and the thermal resistance through the remaining substrate depth is

$$R_{th2} = \frac{\Delta t}{A}(\sigma_{th})^{-1},$$

where Δt is the remaining thickness through the substrate and A is the area of the unit cell. The relative contribution of R_{th2} versus R_{th1} is equal to $r_0\,\Delta t\pi/A$. For example, a 5-μm diode on an (extremely thick) 2000-μm substrate (assume $\Delta t = t$) with a unit cell of 400 μm × 400 μm has an R_{th2} which is approximately 20% of R_{th1}.

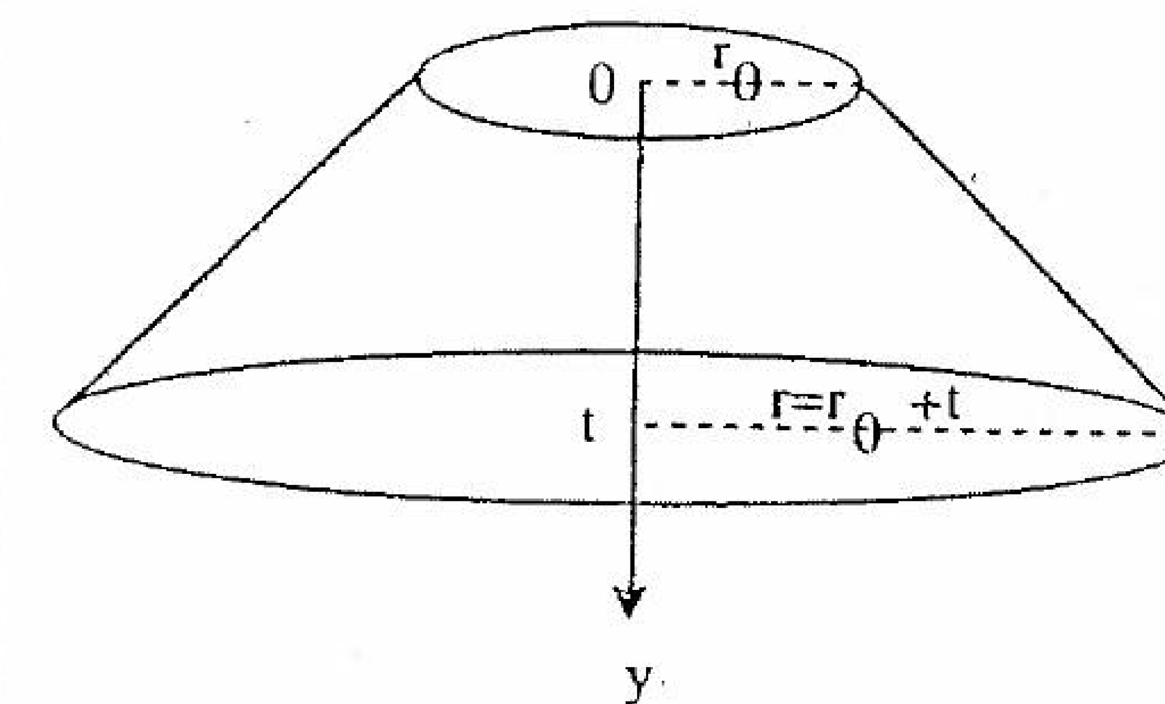


FIGURE 7.12 Assumed heat flow path for a circular diode.

The large amount of heat generated by an array that takes advantage of the inherent high-power capability of the quasi-optical approach is rendered much more manageable by the fact that the heat generation occurs at a large number of evenly spaced low-power heat sources.

One technique that may provide improved thermal performance is epitaxial liftoff [40]. In this technique, the thin active layer of a semiconductor wafer is removed from the substrate and remounted on a substitute substrate possessing desired physical properties. Beryllium oxide (BeO) is an example of a material with the desired high thermal conductivity and low dielectric loss. (The accepted and required handling procedures for BeO, especially with regard to any machining, should be studied and implemented before using this material, because of its toxic properties.) Another possibility is the use of a superstrate layer with high thermal conductivity.

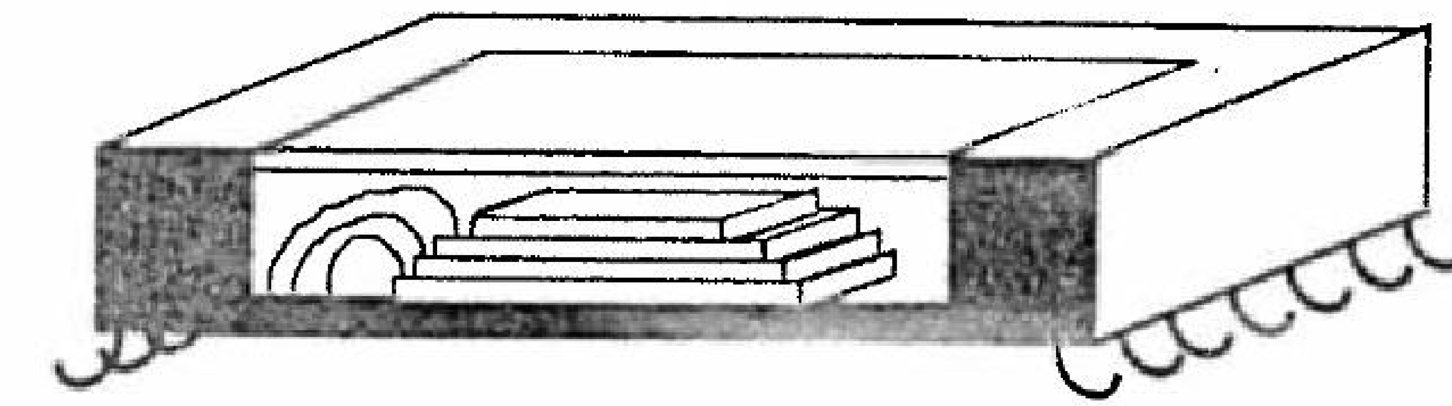
For mechanical reliability, the array must be mounted to a substrate whose coefficient of thermal expansion (CTE) is close to that of the semiconductor material. Without such a match, the array will shatter when subjected to even a slight temperature change. The problem of CTE mismatch increases with increasing size of the chip. Quasi-optical arrays must generally be quite large in comparison with conventional integrated circuits; hence the issue of CTE match is an important one. In addition, due to their high operating power, quasi-optical arrays will likely undergo a substantial temperature excursion during power-up and power-down.

One important consideration in packaging is whether the array is intended as a transmission or reflection grid. Transmission arrays are more difficult to implement, because the transmission side of the quasi-optical path must be transparent. Consequently, the base on which the active array is mounted must be a suitable material (e.g., BeO), and the adhesive by which the array is mounted must be a nonconductive, low-loss material. AlN does not pose the toxicity issue of BeO, and its thermal conductivity is comparable. However, GaAs should not be directly mounted to AlN because of the CTE mismatch.

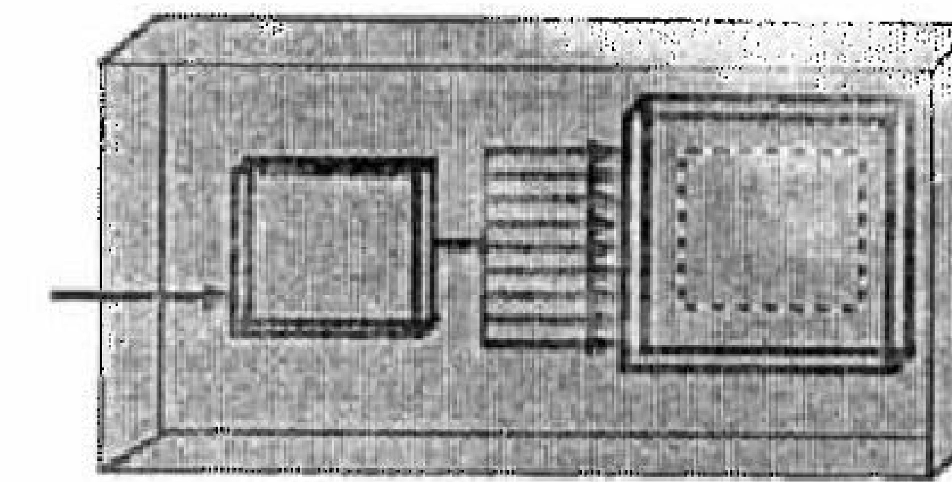
Fused-silica (SiO_2), employed for impedance transformation in previous beam control array circuits, should be used with caution. First, it has a very low CTE (0.5×10^{-6} K^{-1}) and therefore cannot be rigidly attached to GaAs, Si, Al_2O_3, AlN, BeO, and other materials. Second, it has a very low thermal conductivity (approximately 1.2 W $(m - K)^{-1}$). Thus, it will not assist in heatsinking.

Example potential packaging approaches are shown in Figure 7.13. In Figure 7.13(a), a multigrid reflection phase shifter is housed in a ceramic chip carrier. A small air gap is located between the top of the array and inside the package lid to accommodate thermal expansion and contraction in the vertical direction. In Figure 7.13(b), a transmission grid, along with a driver chip, is housed in a multichip module (MCM).

The techniques for electrical attachment on conventional integrated circuits (ICs) are equally applicable to active arrays. The connections will generally be dc or low-frequency ac, however, so microwave wire-bonding techniques need not be employed. Tape automated bonding (TAB) could be considered.



(a)



(b)

FIGURE 7.13 Possible packaging configurations for beam control arrays. (a) Stacked phase shifter in a ceramic chip carrier. (b) Transmission grid integrated with control chip in a MCM.

7.3.6 Alternative Grid Architectures

The discussion has focused on the design of arrays employing integrated semiconductor devices monolithically embedded in a passive grid. A monolithic array directly scaled to lower frequency requires a chip area that increases with decreasing frequency in the relation $A \sim f^{-2}$. A single grid array of reasonable beam size (5λ) will be 1.5 cm $\times$ 1.5 cm at 94 GHz, which may already be prohibitively large for a reliable GaAs circuit. A semihybrid approach in which monolithic arrays are "tiled" together would help circumvent the chip size limitation. However, as a grid array is scaled to lower frequency, the unit-cell size becomes larger and there is much more "open space" between the integrated devices. This is highly wasteful of expensive semiconductor material. In the hybrid approach [21, 41], discrete semicon-

ductor devices or "chip" components containing one or two devices are mounted on and wire-bonded to a low-cost substrate patterned with the passive grid. Hybrid arrays, however, require a great deal of assembly and make array stacking more difficult.

In light of the limitations of both the monolithic- and hybrid-grid approaches at lower frequencies, it is the opinion of this author that the beam control array in its "pure" form of device embedded FSS is only well suited for frequencies above about 90 GHz. To obtain higher "value added" per array element, at low frequencies, an alternative is a quasi-optical power combiner using a more conventional MMIC in conjunction with a separate radiating element (e.g., patch antenna), such as the array in Gouker et al. [42].

7.4 ARRAY CONSTRUCTION

7.4.1 Device Fabrication

Once an array design has been determined, its photomask layout must be created with a computer-aided-design (CAD) program. The predominant data formats used by IC photomask vendors are GDSII (Calma) and CIF. Most layout programs allow output files to be created in one or both of these formats.

Although different in layout and function, the beam control array employing a given electron device uses essentially the same fabrication process as a conventional circuit containing that same device. (Some differences in the metallization steps may be appropriate to accommodate the unique testing requirements for an array and to create the passive metallization grid.). A typical device fabrication process involves photolithographic steps, semiconductor and metal etching, metal deposition, liftoff, and ion implantation. If a foundry process can be used, the array designer's workload is vastly reduced. To fabricate devices, the array designer must first determine the process steps to be employed and the proper parameters for a given step of the process (e.g., ion dosage for implantation). A good source of information on III-V fabrication techniques is Williams's text [43]. For III-V array fabrication, wafers with suitable epitaxial material layers (typically grown by molecular-beam epitaxy, (MBE) must be obtained. Epitaxial growth requires complex and expensive equipment and is typically performed by persons employed specifically for that work. Epitaxial wafers may be obtainable from within the array designer's organization or from a laboratory with which collaborative work can be performed. If such sources are not available, wafers can be purchased from commercial growers. The cost of a (3-in GaAs) MBE wafer from a commercial vendor is $1500–$3000, the price varying according to the difficulty of growing the particular profile.

Indium phosphide (InP) substrate-based materials offer higher performance, epitaxial wafers are much more expensive in InP than GaAs and usually only available in 2-in size. In addition, the fabrication technique is much different, and InP wafers are much more fragile than GaAs wafers.

Fabrication work requires obtaining access to a suitable lab, training in safety procedures, clean-room gowning and particulate control, and detailed training on the specific machines used for the processing. In addition, each fabrication step should be practiced before being attempted on the epitaxial wafer. "Fine-tuning" of the process, based on the results observed in practice fabrication, is almost always necessary.

Key design choices in III-V device fabrication include the technique for creating the Schottky contact and the method of isolation. Schottky varactor beam control arrays fabricated to date have employed the self-aligned aluminum Schottky technique with proton isolation [44]. The self-aligned etched aluminum Schottky process is comparatively simple. Ideally, it is performed on an epitaxial wafer with an aluminum layer grown in situ on top of the semiconductor layers in the MBE machine, although not all MBE growers are willing to perform this extra step. With in situ Al, the Schottky contact surface is formed in the extremely clean environment of the MBE machine, increasing the prospect of fabricating high-quality devices. Etching removes the Al in the undesired areas. Problems observed in the Al Schottky process for PS1 and PS2 arrays included nonuniform etching and unintended etching in later processing steps. In addition, if a layer of Au is used at a later step and contacts the Al, the wafer cannot subsequently be exposed to high temperatures or "purple plague" (Au-Al intermetallic formation) will occur.

Although Al etching has been employed for Schottky varactor beam control arrays because of its simplicity, liftoff is a more mainstream technique. In liftoff, a photoresist layer is patterned onto the wafer and covered with the Schottky metallization. The resist is then removed with acetone. Where the resist was not present, the metal remains, forming the Schottky contacts. Layers of Ti, Pt, and Au (the first for the Schottky, the second as an Au diffusion barrier, and the third as a good electrical conductor) grown successively onto the wafer are most often used. Since photoresist must be patterned before the metal deposition, the Schottky metal cannot be grown in situ if the liftoff process is used. For optical varactors or photoconductive switches, a thin (~ 200 Å) Au Schottky layer is typically employed, which is sufficiently thin to allow light to penetrate. Note, however, that the anode resistance is considerably higher for such a device.

Since the epitaxial wafer is grown with uniform layers of conductive semiconductor material, processing must include an "isolation" step to remove this material everywhere except at the device sites. Two techniques are widely used for isolating III-V materials. (1) In mesa isolation the epitaxial material is etched away except at the device sites. (2) In implant isolation the wafer is bombarded with ions, which become lodged inside the material and neutralize its conductivity. For diode fabrication, implant isola-

tion is very simple, and (proton) implantation has been used in Schottky varactor beam control array fabrication. The device areas are protected from the protons by the photolithographic patterning of a layer of material that serves as an "implant mask." The simplest masking can be performed with a thick photoresist (e.g., Hoechst AZ-P4620). Au implant masks provide much better stopping power but require a much more complicated fabrication.

Isolation implant should be performed at more than one energy to ensure that the implant is spread throughout the doped layers. A two-step implant of 4×10^{14} cm^{-2} at 200 keV and 4×10^{14} cm^{-2} at 100 keV successfully isolated beam control arrays of 1.6- to 1.8-micron-doped layer thickness (including the Al layer, since outside the diode region, the implant must isolate underneath the Schottky metal) with 2–4×10^{18} cm^{-3} n^+ region doping. For Au Schottky contact, the first implant energy should be increased to provide 30 keV per 1000 Å metallization, versus 10 keV per 1000 Å for Al. Although there is some range of successful implant energy and dose, arrays subjected to three times the dosages recommended here were found to have lost most of their C-V transition and were unusable. For InP-based devices, deep isolation implants are not possible; mesa isolation is required.

One critical processing step is that in which the semiconductor material is etched to form the sidewalls of the diode. Wet (chemical) etching has been employed for this step. There will be some lateral etching accompanying the etching into the depth of the semiconductor. Therefore, the actual diode will be narrower than the diode width of the etch photomask. For the PS1 array, diodes drawn to a width of 3 μm shrank to a width of 1 μm, whereas they were expected to shrink to 2 μm. The effect of this on array performance was to shift the center frequency of the array from the intended 99 to 132 GHz! Achievement of predictability in array performance, either through careful calibration of the wet-etch process or by switching to a different etching process, is important for future beam control array development.

7.4.2 Device Testing

Before final array processing, the diodes must be individually testable. For a Schottky varactor, if a reasonable diode C-V characteristic is measured, the device fabrication has been successful (for proof-of-principle experimentation, at any rate). If the isolation were poor, spurious C-V characteristics will be observed due to excessive conduction current. With probe pads attached, however (as for PS1 and PS2), the measured capacitance will be larger than the diode capacitance, since those features contribute an additional fixed capacitance. By cutting sample diodes with a microprobe and subtracting the C-V curve measured after cutting from that measured before, an accurate value of diode capacitance can be obtained. Without this correction, measurements of the PS1 and PS2 diodes overestimated the capacitance by 100%.

The presence of a C-V characteristic on the expected order of magnitude indicates that isolation was successful, but it can be more precisely gauged by current-voltage (I-V) tests. More importantly, I-V tests also serve to identify short-circuited or leaky diodes. Every diode should be I-V tested; or large arrays the testing can be automated by a computer-controlled wafer prober [9]. In Sjogren et al. [9], an HP9836 computer was attached via a general-purpose interface bus (GPIB) to an Electroglas 1034B wafer prober and HP4145 semiconductor parameter analyzer (I-V tester). Short-circuited diodes must be converted to open circuits by microprobe cutting, since a single short-circuited diode will prevent bias from being applied to the entire group of diodes connected when the final (bias) metallization is applied. It is generally advisable to repeat the testing and cutting procedure to ensure that all short-circuited diodes have been found. Testing the PS1 and PS2 arrays was performed several times, until only about five remaining short-circuited diodes were found (and cut) on a 8000–20,000 diode array. A (100-kΩ) series resistor was found necessary to avoid destruction of the diodes by electrical transients from the test system.

For single-ended Schottky diodes with uniform GaAs composition, diode resistance can be measured by driving a large forward current through the diode. In this operating region the exponential behavior of the intrinsic diode current is close to a vertical line on the I-V graph, and the (inverse of the) finite slope of the measured I-V curve represents the deviation from this ideal (i.e., represents the diode RF resistance). With an AlGaAs barrier layer the intrinsic diode curve is flatter, and an accurate measurement of diode resistance cannot be obtained below a current at which the diode is destroyed (approximately 50 mA for PS1 diodes). For the ABD a strictly dc test is not possible, since bias is applied to the individual diodes, not across the RF path. For a pure GaAs ABD it should be possible to measure resistance with a large bias applied to the individual diodes and a small-signal RF applied across the antiseries pair. The actual effective resistance can be determined from millimeter-wave quasi-optical measurements, as described later.

Short circuits occurring after final metallization could be identified by liquid crystal detection [4] or infrared hot-spot detection, although the incidence of such shorts was sufficiently low for the PS1 and PS2 arrays that such a step was not necessary.

7.4.3 Assembly

The PS1 and PS2 arrays were mounted to custom-designed printed circuit boards with household quick-drying glue (Figure 7.11), with conventional wire bonds providing the electrical contact between wafer and board. As discussed previously, practical beam control arrays require more sophisticated packaging techniques.

7.5 MEASUREMENT

7.5.1 Reflection Phase

The most straightforward measurement of array reflection and transmission coefficients is with a network analyzer. Extending the range of commercial network analyzers with frequency multiplication and division may eventually allow their use for the measurement of beam control arrays even into the upper-millimeter-wave region. Due to the lack of availability of such instruments up to now, however, quasi-optical network analysis techniques have been developed in tandem with beam control arrays.

A reflection phase measurement was performed by Lam et. al. [4] by placing the array behind an aperture in a plate covered with microwave absorber. The power reflecting from the absorber-covered plate was used as a reference reflected beam. Since the reflectance from the absorber is low, but the beam reflects over a large area, this reference beam is of comparable strength to the signal beam from the array. From a sequence of measurements taken with the array translated in the quasi-optical path by one-eighth wavelength, the amplitude and phase of the reflected beam relative to those of the reference beam can be extracted.

A major problem in reflection coefficient measurements is to eliminate "garbage" reflections from regions adjacent to the active portion of the array. This was ingeniously addressed by Lam et. al. by use of the "garbage" itself as the reference beam [4]. Although this allows the array to be tested, in actual operation only the phase-controlled beam can be allowed to reflect. Roberts and Compton [45] take a similar phase measurement approach, but now the reference wave is obtained from a power splitter at the source, with only the array present in the quasi-optical path. Since this method was employed with a passive FSS, peripheral hardware from which "garbage reflections" would occur is not present.

Recently, a lens-focused approach was successfully employed to obtain very precise scalar reflection coefficient measurements [46]. A lens-based approach for phase measurement, inspired by this work, proved successful as well [47]. Although the beam impinging on the array under evaluation is a Gaussian of perhaps as little as 1 λ beam waist radius, the results nevertheless agree with those of a plane-wave (transmission line) analysis. In the method of Sjogren et al. [47] the polarization sensitivity of the array is employed to measure the reflection phase. With an incident beam tilted with respect to the axes of the diode embedding strips and bias lines of the array, a portion of the beam is polarized to the axis for which the array provides a fixed (bias-independent) reflection. This component is used as a reference beam. The polarization state of the resultant reflected beam is employed to extract the phase of the "active axis" beam relative to that of the orthogonal "passive axis" beam. An advantage of this technique is that it provides a "semiabsolute" phase, as opposed to the relative phase obtained by the other reference-wave techniques. Since the reflection coefficient of the passive-axis beam for the beam control array is one of a simple inductive grid, it can be determined analytically to good accuracy. To the extent that it can be treated as a "known," the absolute phase of the active-axis beam is consequently known. Determining absolute phase by other techniques requires calibration testing with the beam control array replaced by a reflector at precisely the same reference plane. To perform such a calibration at millimeter-wave frequencies requires extreme mechanical precision, which is not necessary with the polarization technique. Figure 7.14 shows the experimental configuration for testing reflected beam phase by polarization. The relative phase of a beam with electric field polarized to the active (y) axis versus that polarized to the orthogonal transverse axis (x) is

$$\phi_{yx} = \arcsin\left\{\frac{\sin[2\arctan(\pm E_{\min}/E_{\max})]}{\sin[2\arctan(E_{0y}/E_{0x})]}\right\},$$

where $E_{\max}$ and $E_{\min}$ are the maximum and minimum electric-field amplitudes of the polarization ellipse, respectively, and E_y, and E_x are the active-axis and passive-axis electric-field amplitudes, respectively. (Note that a diode detector signal is normally proportional to power, so the square root must be taken to obtain the relative field strengths.) If the receiver horn, adjusted to the angle at which the reflected field is maximum ($E_{\max}$), points in the same quadrant as the source horn, then ϕ_{yx} lies in the range $\pm[0, \pi/2]$, whereas if it points in the orthogonal quadrant, ϕ_{yx} lies in the range $\pm[\pi/2, \pi]$. The technique determines the phase within a range of

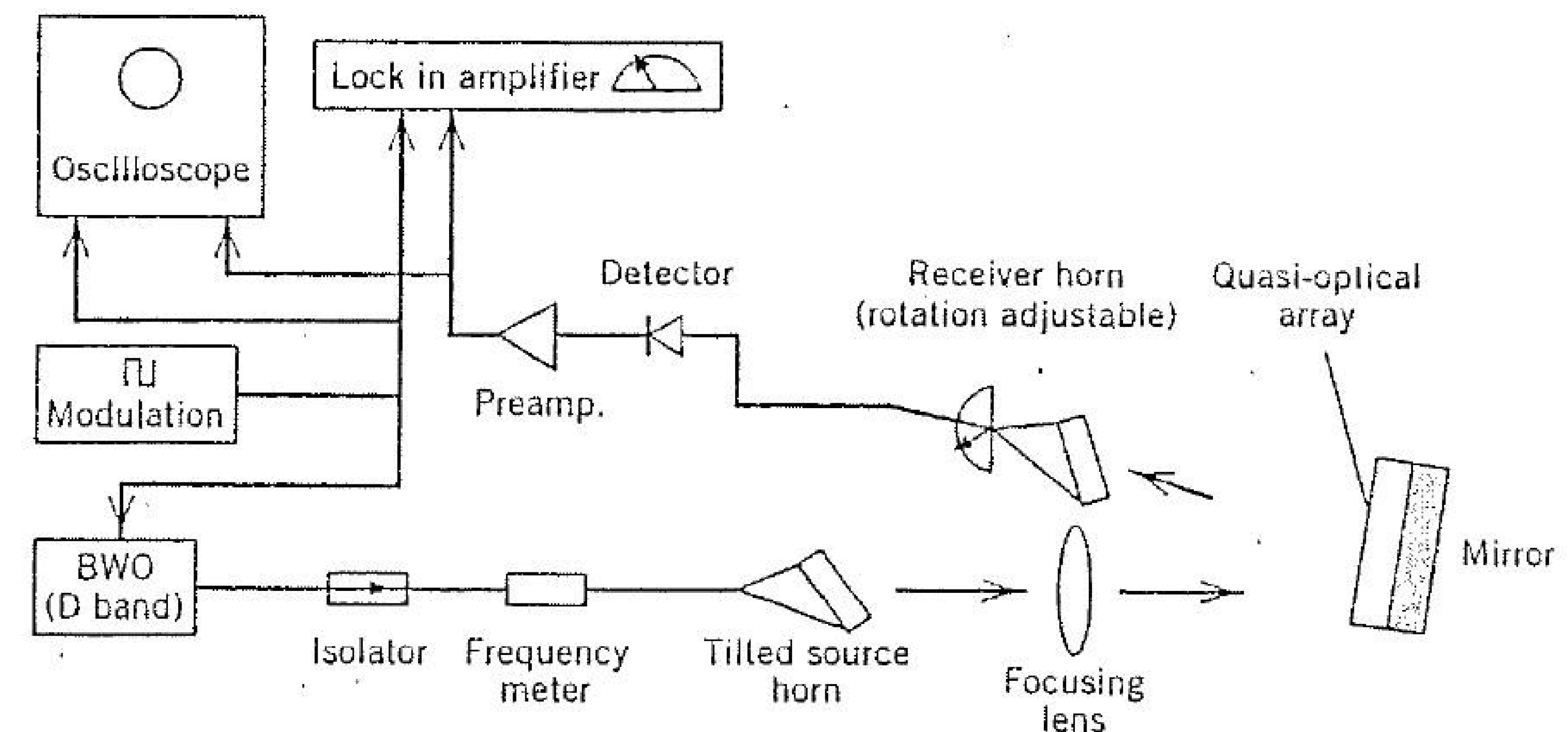


FIGURE 7.14 Configuration for reflection coefficient phase measurement by the polarization technique [47]. (©1992 Wiley.)

180°; the sign of the phase must be determined by comparing the experimental and predicted results. The technique described can be employed for either reflection or transmission phase measurements.

7.5.2 Reflection Amplitude

In principle, all of the discussed phase measurement techniques employing a reference signal are capable of providing the amplitude of the signal beam relative to the amplitude of the reference beam. For phase, a reflector can be used as a calibration standard. In contrast to phase measurement, amplitude measurement is not strongly affected by a slight translational error in mirror position. However, the planes in which the quasi-optical device and calibration reflector are successively placed must be highly parallel to avoid shifting the reflected beam angle. In PS1 array testing the required precision was difficult to achieve without extensive additional fixturing. Therefore, an alternative approach was taken to measure amplitude. This approach relies on the fact that the substrate thickness is a multiple of a half-wavelength at certain frequencies. At these frequencies, the back-reflecting mirror should short-circuit the array plane so that no power is absorbed by the array. Thus, the amplitude measured at one of these frequencies should serve as a unity-reflectance reference. If the array passive axis is lossless (a reasonable but not exact approximation because of the metal-strip resistance), measurement of a passive-axis beam component at the frequencies under test provides a measurement of the relative source power versus frequency. The active-axis beam measured at the $m\lambda/2$ frequency provides the unity reference for the active-axis beam. This technique is limited to a frequency range over which the beam power pattern does not vary appreciably.

It would appear that an even simpler amplitude measurement should be possible with the polarization measurement technique. With a given tilt angle of the source horn, the relative power of the active- and passive-axis beams should be governed by simple trigonometry. With the passive-axis beam serving as a reference, the relative power of the active-axis beam should determine the amplitude of the reflected beam. For reasons not fully understood, this approach did not provide an accurate result. It appears that amplitude measurements are much more susceptible to mechanical imprecision of the experimental setup than are phase measurements. This approach may still prove workable if it is performed with greater precision.

7.5.3 Transmission Amplitude/Phase

In general, transmission testing is easier than reflection testing. For the PS1 array, the transmission coefficient was measured by placing the array behind an aperture in an opaque obstacle (metal sheet covered with microwave absorber). The measurement configuration is shown in Figure 7.15.

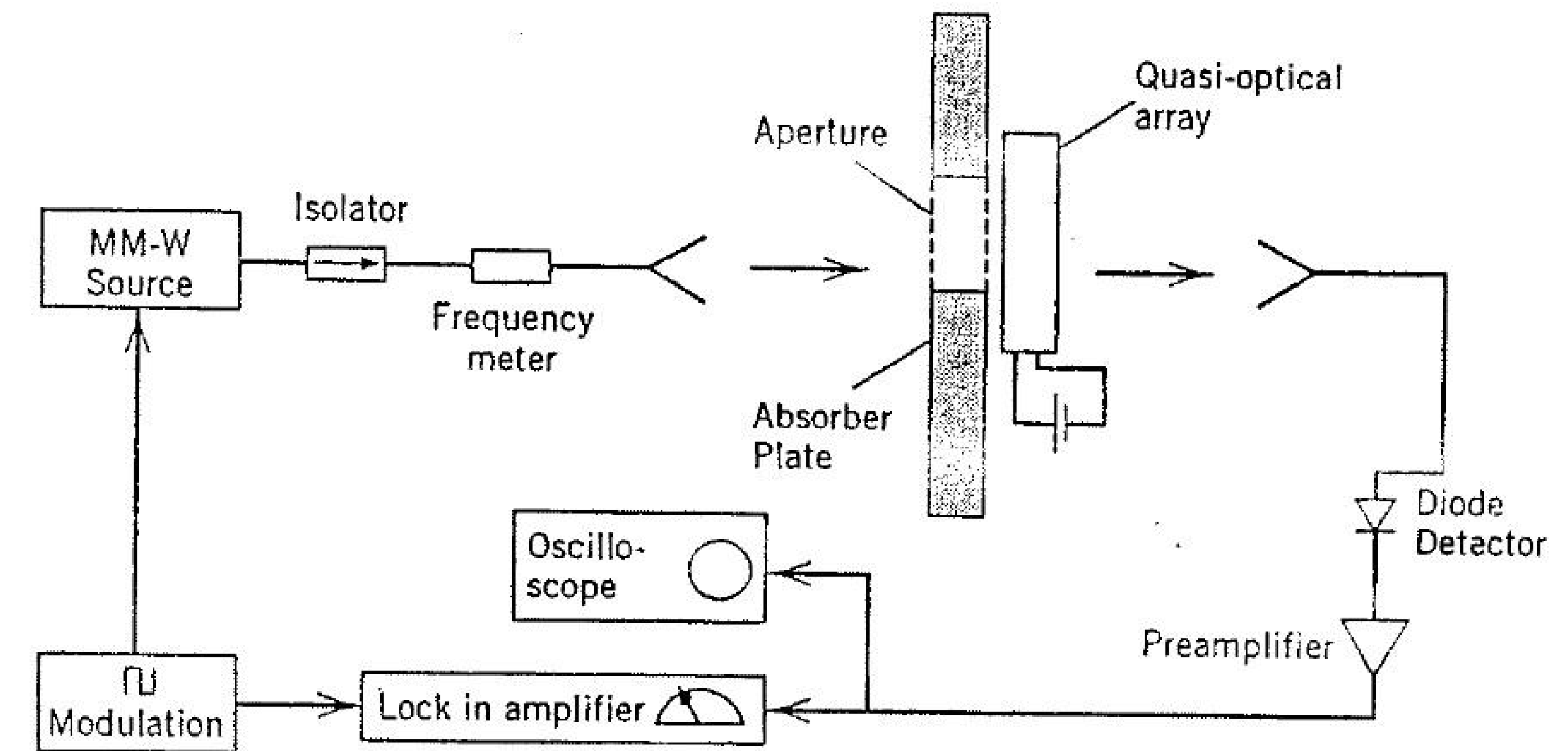


FIGURE 7.15 Configuration for transmitted amplitude testing of a beam control array [10]. (©1993 IEEE.)

The measured power with the array absent was used as the unity-transmittance reference. Standing waves between the grid and the source or receiver horn must be avoided. One way is by tilting the array normal axis slightly (perhaps up to 10°) from the beam propagation axis. The theoretical grid impedance changes little with such a tilt.

As mentioned, transmission phase can be measured using the polarization technique.

7.5.4 Characterization

It is clear from the experimental results described that the series-resonant varactor diode array is a versatile control component for quasi-optical applications. As for any other high-frequency electronic or electromagnetic hardware, physical nonidealities cause the actual array performance to differ somewhat from the simulated performance. For the beam control diode array these variances are due to the variability of effective diode size across the array, variation of series resistance, and the faulty array cells.

To refine the simulation model, it is desirable to extract model parameters from experimental results. This can be done by procedures similar to those used to characterize discrete semiconductor devices. Since a good circuit model is closely related to the physical structure of the device it represents, knowledge of the values for the model elements assists in developing an improved device. In addition, a good model is essential to apply the device to other circuits and operating conditions (e.g., frequency).

The model parameters of microwave devices are typically extracted from S-parameter measurements with the device embedded in a one- or two-port

TABLE 7.2. Model Parameters of Demonstrated Arrays [48]©1995 IEEE

Design	C_{min}(fF)	c_{rd}	η_{q0}	R_{array} (Ω)
[4]	17.5	3.29	0.630	78, 26
PS1	4.9	6.35	0.395	35
PS2	4.7	5.12	0.613	75

calibration fixture. The model parameters of beam control arrays have been successfully extracted in the same manner from "quasi-optical S-parameter" (reflection and a transmission coefficient) measurements. The circuit element values are chosen as those that, employed in simulation, give results that match the measured results. The PS1 array parameters were extracted from complex transmission coefficient measurements [10]. Transmitted beam phase was measured by the polarization technique. Since parasitic capacitance was suppressed by the rectangular unit-cell design, the array model was assumed to be representable as a simple three-element series RLC circuit. A similar parameter extraction procedure was employed on the PS2 array, but with reflection rather than transmission coefficient measurements [48]. In both cases the empirically derived models provided a good representation of array behavior. Table 7.2 summarizes the parameters of beam control arrays demonstrated so far. The minimum capacitance, C_{min}, provides a comparative measure of the operating frequency capability of the array. The diode capacitance ratio $c_{rd} = C_{max}/C_{min}$ is a gauge of the performance range of the diode. The quasi-optical efficiency, η_{q0}, is the ratio of array capacitance to diode capacitance and represents the degree to which the diode performance is translated to the array as a whole. The array resistance, R_{array}, provides a gauge of the power loss incurred by the array.

7.6 ALTERNATIVE CONTROL TECHNIQUES

Different mechanisms exist for achieving external control of a quasi-optical array. Figure 7.16 shows those identified thus far that appear to be of practical interest.

Initial experimentally demonstrated beam control arrays have achieved the control function through externally applied voltage bias. In a recent demonstration a photodiode array demonstrated variable beam transmittance under optical control [49]. In this array, light incident on the photodiodes serves to modify their capacitance, as the incident voltage does for the conventional beam control array.

In another experiment, the bias lines of a voltage-controlled array were optimized for high-speed guided-wave propagation. Initial results show operation at 1 GHz without appreciable output degradation [50]. This represents a factor of 10 improvement over the speed obtained in earlier work [10].

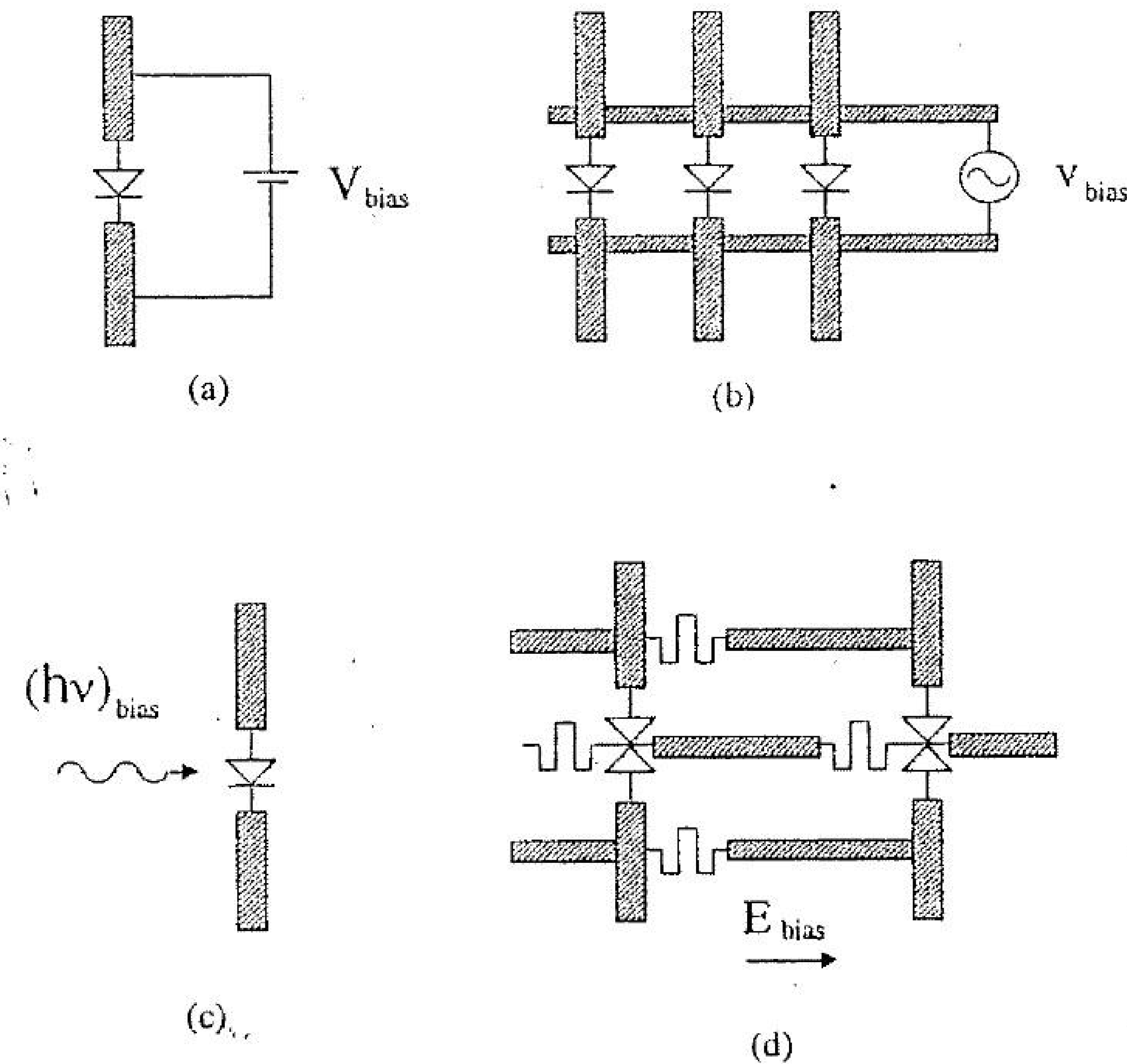


FIGURE 7.16 Alternative array control mechanisms: (a) dc/low-frequency control; (b) RF/guided wave control, (c) Optical control; (d) Quasi-optical control.

An additional potential control technique is "quasi-optical" bias [30]. This technique relies on the fact that the beam control array operates on a beam polarized to a single axis. For the standard beam control array the other axis allows the presence of bias lines with little effect on array behavior. In quasi-optical control an array design would employ a quasi-optical beam polarized to the other axis as the control signal. Some considerations for the design of such an array are given in Sjogren et al. [30].

In general, these alternative control techniques offer the potential for very high control speed. An application illustrating the usefulness of such higher speeds is the quasi-optical Q switch [30]. Here, a beam-switching array is used as a "dam" to store power within a quasi-optical Fabry-Perot cavity. When the array switches the cavity to a low-Q state, the stored energy is released with a peak power potentially much higher than the instantaneous power of the continuous-wave source providing the energy to the cavity. Thus, such arrays have potential application in high-power pulse generation.

ACKNOWLEDGMENTS

The author wishes to thank Professor Neville C. Luhmann, Jr., under whose direction the PS1 and PS2 beam control arrays were developed. Refinements of some of the concepts developed and the development of new concepts have been performed as unsponsored, independent work on the part of the author.

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CHAPTER EIGHT

Quasi-Optical Grid Arrays

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To make high-frequency electronic devices, one needs to be able to control tolerances to a small fraction of a wavelength. In the millimeter-wave band this is on the order of a few microns, a size sufficiently small that the fabrication of conventional microwave circuits becomes both difficult and costly. Consequently, alternative techniques based on quasi-optics are a sensible and practical approach at these frequencies. Quasi-optics allow the mature technology of optics to be scaled down to operate in the microwave and millimeter-wave bands. These techniques promise greater power and performance in the millimeter-wave band than is presently achievable with conventional circuit designs.

8.1 QUASI-OPTICAL POWER COMBINING

Quasi-optical power combining is an efficient method of coupling many devices together. Quasi-optic circuits look very different from conventional microwave and millimeter-wave combining circuits. A traditional microwave combiner is based on transmission lines, frequently waveguide or microstrip, and lumped-element circuits with the devices electrically connected to the combining circuit with metal conductors. Such structures exhibit significant limitations as the frequency of operation increases. They are subject to

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conduction and radiation losses that degrade efficiency, their fabrication becomes complex and expensive due to the small size of the circuits at high frequencies, and they are unsuitable for combining more than a few devices. Their small size also makes them relatively fragile and unreliable.

Quasi-optical power combining eliminates these problems by coherently combining the outputs of many devices in free space. By eliminating the metal walls found in waveguide systems, quasi-optic systems reduce sidewall conduction losses that can reduce efficiency in waveguide combiners. Through the use of dielectric slabs, polarizers, metal-patterned grids on substrates, and surfaces embedded with hundreds of individual solid-state devices, microwave components synthesized quasi-optically behave similarly to conventional lumped circuit elements and transmission lines but with much greater power-handling capabilities. However, unlike conventional circuit elements, quasi-optical components have dimensions that are large compared to a wavelength, thereby avoiding the fabrication problems that plague conventional circuits designed to operate in the millimeter-wave band.

Although quasi-optical circuits look like optical devices (Figure 8.1), they can be modeled with reasonable accuracy with simple transmission line and lumped-element components. This has the fortunate consequence that the immense knowledge and sophisticated computer-aided design tools developed for conventional microwave circuits can be readily applied to the design and modeling of quasi-optical circuits. In addition, active quasi-optical circuits are often highly suited for manufacture by planar photolithographic techniques commonly used by the semiconductor industry. This significantly

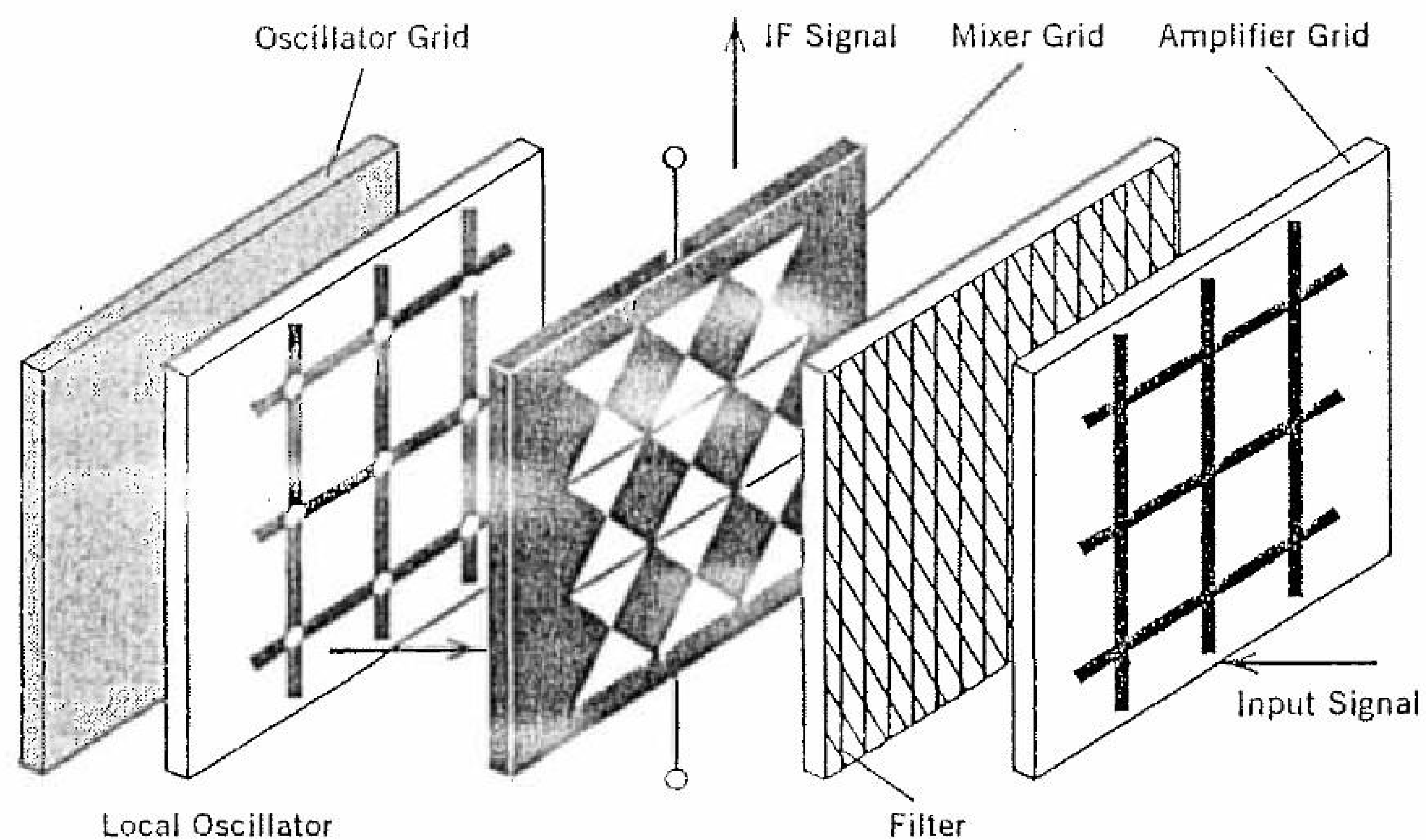


FIGURE 8.1 A quasi-optical receiver.

decreases the capital expenditure required to implement quasi-optical systems and allows seamless integration of quasi-optic components into existing semiconductor fabrication processes.

8.2 EQUIVALENT CIRCUIT MODELS FOR PLANAR GRIDS

Modeling the electromagnetic properties of quasi-optical grid components is a difficult yet essential task if quasi-optical systems are to be reliably designed. Scattering from periodic structures can be determined rigorously by the method of moments [1–4]. However, a drawback of this approach is that a relatively complicated set of equations is generated that must be solved numerically. Other numerical techniques, such as the finite-element method [5] or conjugate method [6], use an iterative approach that can require the computational resources of a supercomputer. For these reasons it is often the case that approximate methods based on equivalent circuit models (ECMs) are a convenient alternative to the more rigorous analysis techniques when applied to periodic grids.

One particularly useful analysis technique for determining the ECMs for periodic grids is the induced electromotive force (EMF) method. This method, introduced by Brillouin in 1922 [7] and developed by Carter [8], was originally used for calculating the self-impedance of various antennas. Tai applied the method to find the impedance of a biconical antenna [9] and Elliot [10] applied it to a center-fed dipole. Eisenhart and Khan [11] extended the technique to waveguides and used it to derive the impedance of a waveguide mounting structure.

Application of the EMF method relies on knowing how the currents on a given radiating structure are distributed. As a result, it is primarily used for simple configurations on which the current distribution can be assumed with reasonable accuracy. The relation between an impressed current, $\mathbf{J}(\mathbf{r})$, and the resulting electric field, $\mathbf{E}(\mathbf{r})$, is given by the inhomogeneous wave equation

$$\nabla \times \nabla \times \mathbf{E}(\mathbf{r}) - k^2\mathbf{E}(\mathbf{r}) = j\omega\mu\mathbf{J}(\mathbf{r}), \tag{8.1}$$

where $k = \omega\sqrt{\mu\epsilon}$. The solution of this equation determines the fields produced by the currents on a radiating structure. Usually this involves the dyadic Green's function, $\overline{G}(\mathbf{r}|\mathbf{r}')$, for the structure. The solution is

$$\mathbf{E}(\mathbf{r}) = -j\omega\mu\int_V \overline{G}(\mathbf{r}|\mathbf{r}') \cdot \mathbf{J}(\mathbf{r}')\, dv', \tag{8.2}$$

where the primed coordinates denote the region containing the impressed current distribution.

Once a current distribution is assumed and the resulting fields found from Eq. (8.2), Poynting's theorem is applied to determine the power radiated. Poynting's theorem for phasors is normally stated as

$$\oint_S \mathbf{E} \times \mathbf{H}^* \cdot d\mathbf{s} = -\int_V \mathbf{E} \cdot \mathbf{J}^* \, dV - j\omega \int_V (\mathbf{H}^* \cdot \mathbf{B} - \mathbf{E} \cdot \mathbf{D}^*) \, dV. \quad (8.3)$$

For the EMF method, the driving-point impedance, Z, is calculated by equating the power delivered to Z with the total complex power radiated. As a result, the impedance is

$$Z = -\frac{1}{|I|^2} \int_V \mathbf{E}(\mathbf{r}) \cdot \mathbf{J}^*(\mathbf{r}) \, dV, \quad (8.4)$$

where $|I|$ is the magnitude of the assumed current distribution at the feed point.

Finding the embedding impedance for solid-state devices integrated into a periodic grid is similar to determining the input impedance for an antenna or waveguide mounting structure. The general task of calculating the driving-point impedance for devices in a finite grid is difficult. Complications arise from the unknown behavior of the field at the grid edges. In addition, each device in the array will couple to all other devices through the radiated fields. Even grids of moderate size generate a large number of unknowns that can make analysis exceedingly difficult. To make the problem more tractable, one usually assumes that the grid is infinite in extent. Under this approximation, edge effects are ignored. The problem can be simplified further if the grid has internal symmetries that can be exploited.

For many grid structures it is common to find planes of symmetry that leave the grid unchanged with respect to reflection. The simplification that results from this internal symmetry is illustrated in Figure 8.2. Each grid cell is assumed to contain an identical ac current source. Furthermore, it is assumed that these current sources are locked to a single phase. This situation represents an array of phase-locked oscillators, which is the basis for a quasi-optical power-combining grid. Symmetry planes running horizontally can be replaced with electric walls. This results because identical currents flow above and below these planes, thus canceling the tangential electric field. Similarly, vertical symmetry planes can be replaced with magnetic walls. Once again, these arise from image currents. In this way an infinite grid of phase-locked sources can be represented by an equivalent waveguide or unit cell. The equivalent waveguide has electric walls on the top and bottom and magnetic walls on the sides (Figure 8.3). This equivalent waveguide representation is valid whenever a transverse electromagnetic (TEM) wave is radiated from or incident on the grid. A plane wave incident

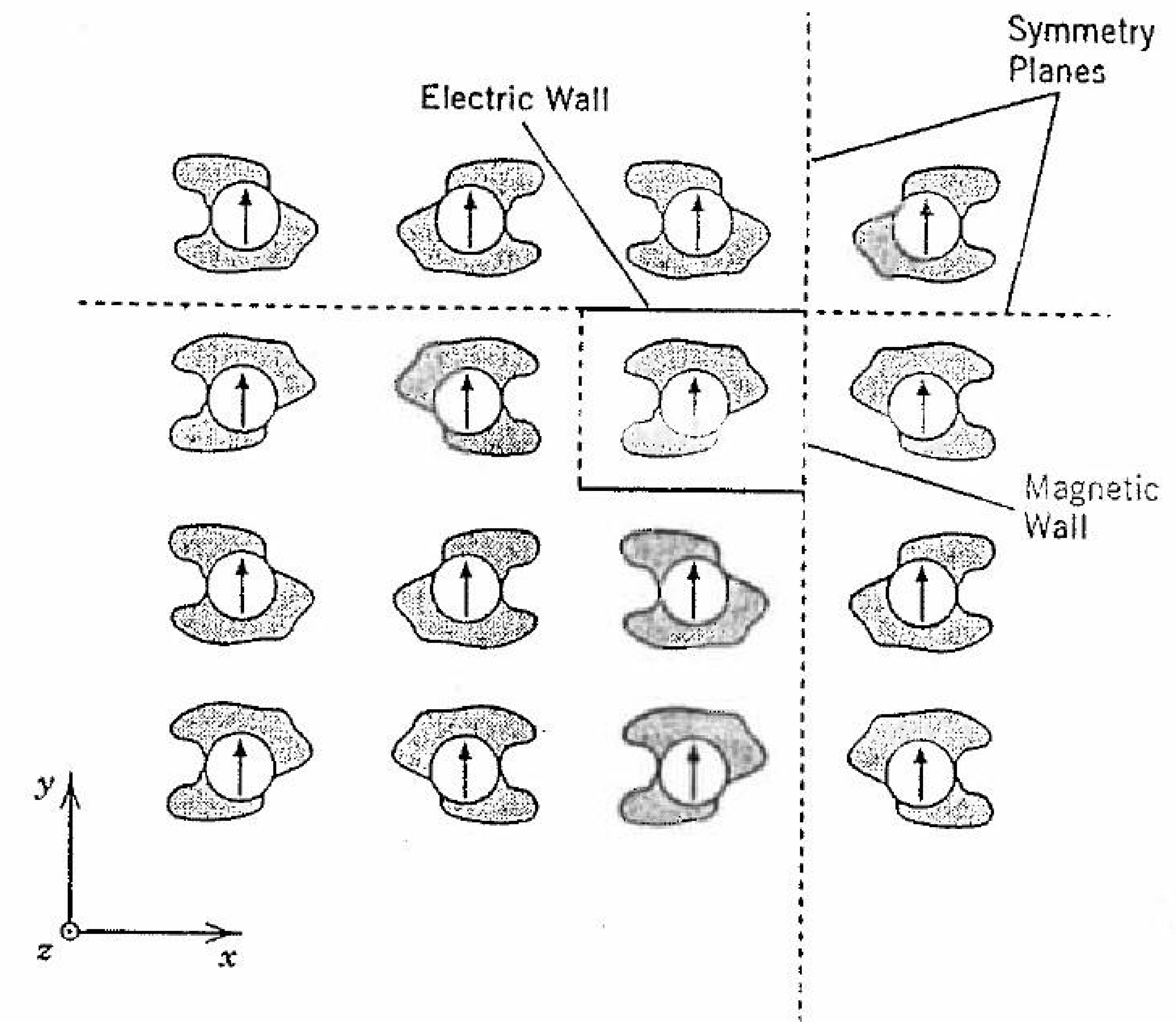


FIGURE 8.2 Schematic of a planar grid with reflection symmetry. Two symmetry planes are shown with dotted lines. If each cell is excited with an identical source, then horizontal symmetry planes can be replaced with electric walls and vertical symmetry planes with magnetic walls.

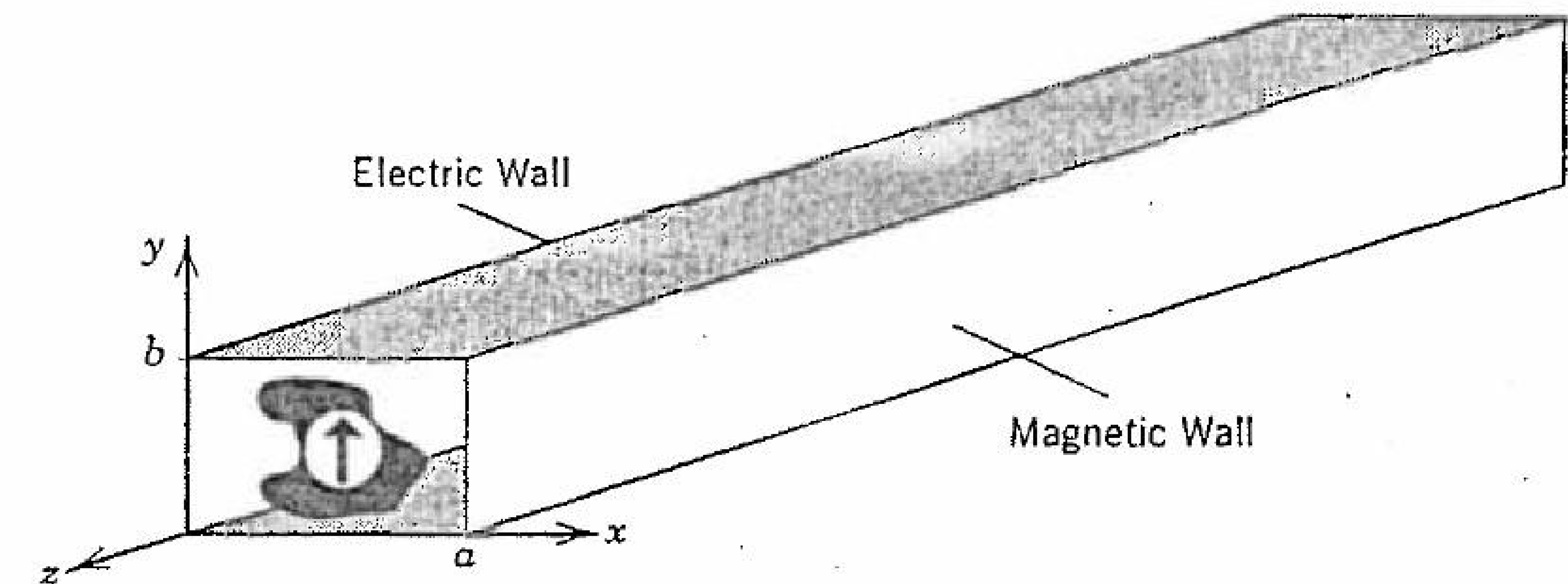


FIGURE 8.3 The planar-grid equivalent waveguide. The waveguide has electric walls on top and bottom and magnetic walls on the sides.

from the z direction with the electric field polarized along the y axis will induce currents on the grid surface. As before, these currents will be in phase, allowing the grid to be represented by an equivalent waveguide.

Because the EMF method uses an assumed current, it is not as accurate as more rigorous techniques, such as the method of moments (MOM). Usually, the assumed current is chosen to have a very simple form, such as a uniform distribution. Quasi-optical measurements on a variety of grids have indicated that impedance calculations using such assumptions tend to give quite reasonable results (within 10% of theory) if the structure being analyzed is smaller than a wavelength [12]. The reason for this is that impedances calculated from the EMF method using real sources are stationary with respect to small variations in the source distribution. Thus, even if an assumed current distribution on the structure is good only to first order, the impedance calculated from that distribution tends to be accurate to second order [13]. For very accurate modeling, however, accurate current distributions, such as those obtained from MOM techniques, are required.

In addition to giving a reasonable and simple approach to modeling quasi-optical arrays, the EMF method permits the effect of dielectric substrates, slabs, and planar mirrors to be included in a convenient way. For a grid the driving-point impedance is expressed as a sum over equivalent waveguide-mode impedances. Each of these mode impedances is a parallel combination of the mode impedance looking in the $+z$ and the $-z$ directions. The mode impedance looking in a particular direction may be calculated using transmission line theory [14]. Substrates, various dielectric slabs, and planar mirrors are taken into account by treating them as transmission lines and shunt short-circuited stubs *for each mode*. The intrinsic impedance and propagation constant appropriate to each waveguide mode can then be used along with transmission line theory to determine the total mode impedance looking in that given direction from the surface of the grid.

So far, we have assumed normal incidence in our analysis. Although the EMF method can be applied to nonnormal incidence, the equivalent waveguide boundaries are no longer simple magnetic and electric walls. Fortunately, for power-combining grids, we are usually interested in broadside radiation and can neglect the nonnormal case. Nevertheless, grids are multimode devices and preserve the angle of incidence for an incoming signal. This has been demonstrated with a grid amplifier, where it was shown that the grid amplifier preserved the direction of the incident beam [15]. However, the impedances calculated from the EMF method, under the assumption of normal incidence, are no longer valid.

Planar periodic grids are well suited to the EMF method if the grid structure has a simple symmetric geometry and the periodicity is smaller than a wavelength. An EMF analysis is applied to the equivalent waveguide to find the grid embedding impedance. This embedding impedance may be represented as a transmission line circuit that describes the coupling between a device placed in the grid and a TEM wave.

8.3 GRID OSCILLATORS

A quasi-optical grid oscillator consists of a two-dimensional periodic array of active devices producing a planar sheet with a reflection coefficient greater than unity. A resonator can be used to provide feedback to couple the devices to form a high-power oscillator (Figure 8.4). By integration of many devices into the grid, very large powers can be achieved despite the inherent lower output power of solid-state devices operating in the millimeter- and submillimeter-wave bands. The planar configuration of the grid is suitable for monolithic integration and provides an attractive means of obtaining high power from solid-state devices that is scalable to millimeter-wave frequencies.

Two important features distinguish grid oscillators from most quasi-optical power combiners built from microstrip circuits. First, grid oscillators do not necessarily have a ground plane and, as a result, do not rely on the interaction of microstrip modes with free-space radiation. Second, microstrip-based power combiners tend to be a collection of individual free-running oscillators that are weakly coupled. Thus, the operating frequency depends primarily on the behavior of the individual oscillators. In contrast, the elements making up a grid oscillator are not themselves free-running oscillators. Mutual interaction of all the devices in the grid is necessary for oscillation to occur. Consequently, the oscillation frequency and output power are strongly affected by device spacing and grid configuration. Each device in the array is presented with an embedding impedance that is a

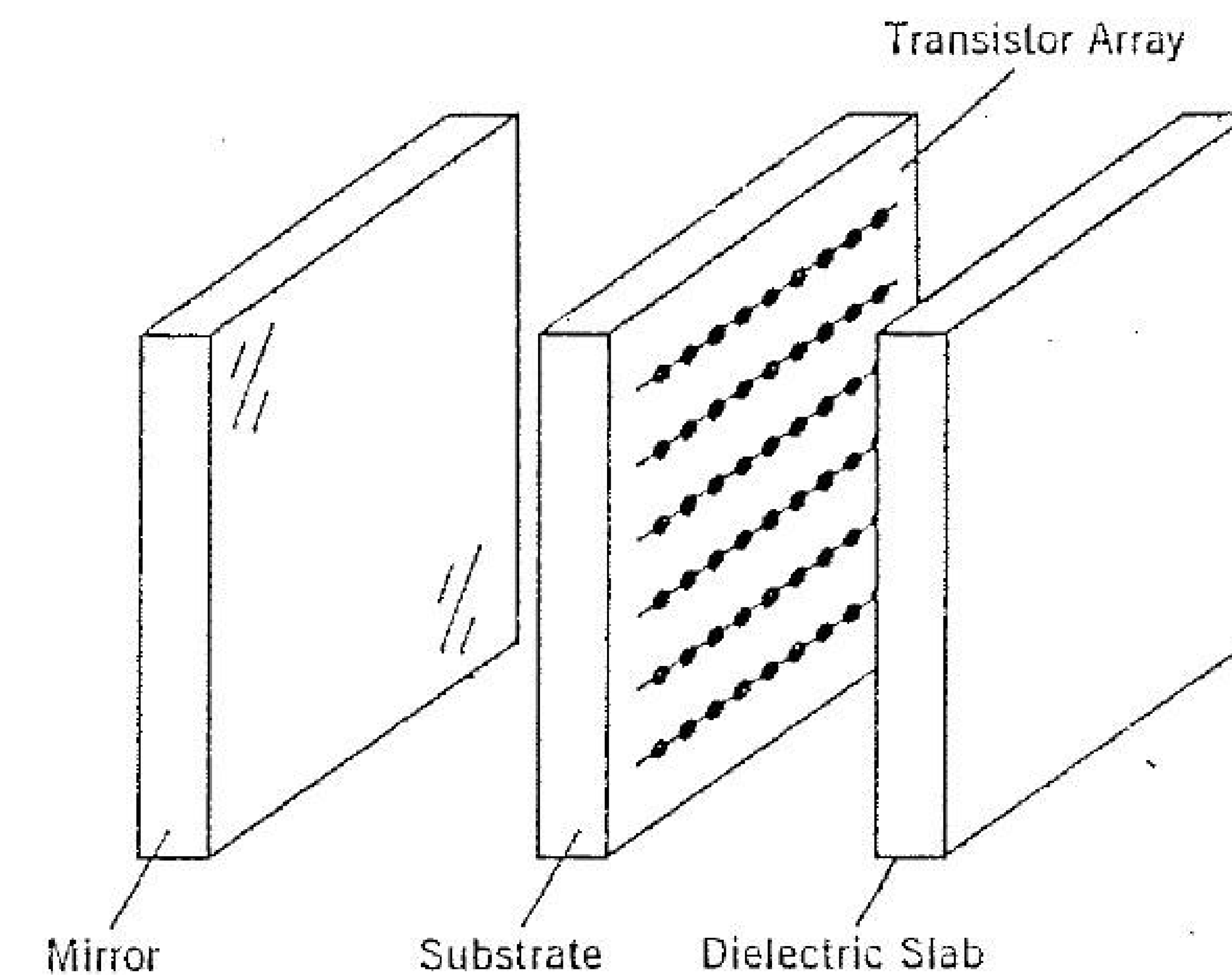


FIGURE 8.4 Schematic of a grid oscillator. Active devices are embedded in a two-dimensional periodic array supported by a dielectric substrate. The grid array is placed in a Fabry-Perot cavity that couples the devices.

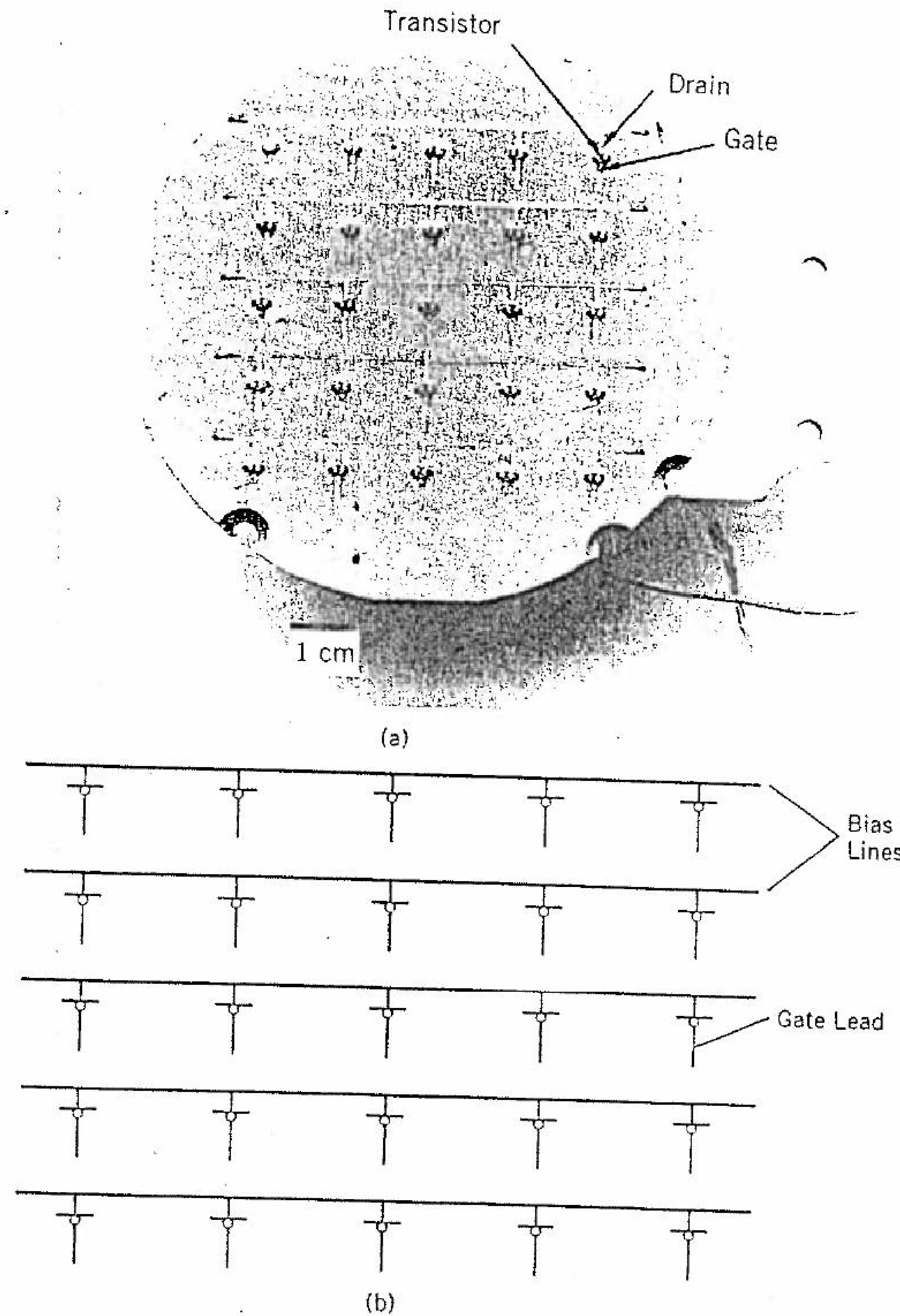


FIGURE 8.5 (a) A 25-element MESFET grid oscillator. The backside of the substrate is metallized, and a dielectric slab is placed in front of the grid to form a Fabry-Perot cavity. (b) Grid configuration. The MESFET drain and gate are connected to the vertical leads. The source leads run through the substrate and are soldered to the ground plane.

function of the grid structure. This embedding impedance, together with the device impedance, determines the grid's overall behavior as an oscillator.

In principle, any solid-state device can be used in a grid oscillator. Although readily amenable to planar integration, two-terminal devices generally have poor dc-to-RF (radio frequency) efficiencies. Experimental Gunn diode grid oscillators have proven difficult to synchronize as well. Transistors, on the other hand, have respectable dc-to-RF conversion efficiencies and a separate control terminal. This allows the devices to be more easily stabilized, permitting oscillation to be controlled through an appropriately designed feedback circuit.

A variety of transistor grid configurations has been investigated. The first demonstrated transistor oscillator grid is shown in Figure 8.5(a) [16]. The array was fabricated on a Duroid dielectric substrate. Packaged metal-enhanced semiconductor field-effect transistors (MESFETs) were soldered into the grid. The vertical metal lines, which were connected to the transistor drain and gate terminals, are parallel to the radiated electric field. Horizontal metal leads running across the grid were used for dc biasing. The backside of the substrate was metallized and served as both a mirror and ground for the MESFET source leads. Figure 8.5(b) shows details of the grid configuration. The device spacing was 13 mm. The gate, which was connected to a 5-mm-long inductive strip, was not dc biased. When dc bias was applied to the drain, the grid oscillated at 9.7 GHz. The metallized backside of the substrate and a quarter-wave-thick planar dielectric slab placed in front of the grid formed a Fabry-Perot resonator. Varying the distance of the front dielectric slab tuned the frequency about 1% and the output power by nearly 10%. The total radiated power, calculated by measuring the far-field radiation pattern, was 464 mW. This corresponds to an effective radiated power (ERP) of 20.7 W and a dc-to-RF conversion efficiency of about 15%.

An attractive feature of grid oscillators is the ability to model them with relatively simple transmission line circuits. Figure 8.6 shows an example. Energy radiated from the grid is modeled as a wave propagating along a transmission line. The characteristic impedance of the transmission line corresponds to the TEM impedance for a wave traveling in that dielectric medium. Thus, for the grid of Figure 8.5(a), free space is represented with an $\eta = 377\text{-}\Omega$ transmission line, and the dielectric slabs are modeled with

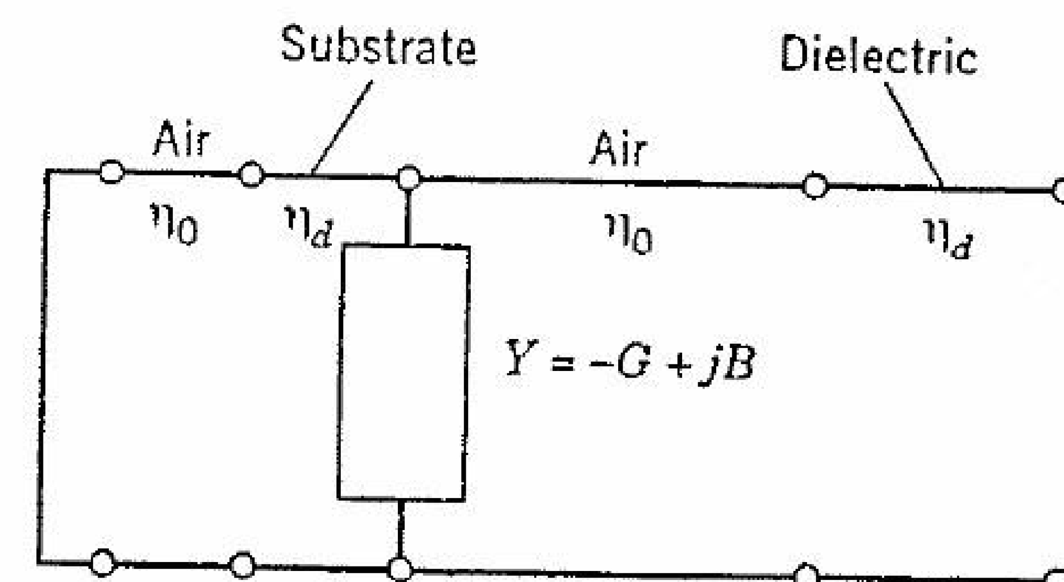


FIGURE 8.6 Generic transmission line model for a grid oscillator. Radiated power is represented as a wave traveling along a transmission line.

$\eta_d = 377/\sqrt{\epsilon_r}\ \Omega$-lines. A short circuit models the mirror behind the grid. A shunt admittance, Y, represents the devices and the embedding impedance. This admittance is a function of the grid configuration as well as the impedance of the embedded devices. For a grid containing active solid-state devices, the real part of the admittance is negative.

8.3.1 Bar-Grid Oscillators

An alternative quasi-optical grid configuration is shown in Figure 8.7. The grid consists of an array of metal bars on which devices are mounted. This structure has been used to combine the output powers of both transistors [17] and Gunn diodes [18]. A mirror placed behind the grid couples the devices and is used for reactive tuning. The metal bars, which provide dc bias to the devices, make an excellent heatsink. For convenience, the devices in adjacent rows share dc biasing. This arrangement minimizes the number of biasing connections. It also gives the grid a symmetric structure that can be exploited to determine the grid's embedding impedance.

A transmission line model, similar to that shown in Figure 8.6, is used to describe the bar grid. Each device in the grid is viewed as occupying a unit cell defined by symmetry. If the devices in the grid are identical and all are oscillating in phase, the electric and magnetic fields must satisfy symmetry-imposed boundary conditions along the edges of the unit cell, forming an equivalent waveguide as illustrated in Figure 8.7(b). A device placed in the grid is viewed as a source that excites the equivalent waveguide. A transmission line model representing the MESFET bar-grid oscillator is shown in Figure 8.8. The drain and gate leads excite different waveguides formed by

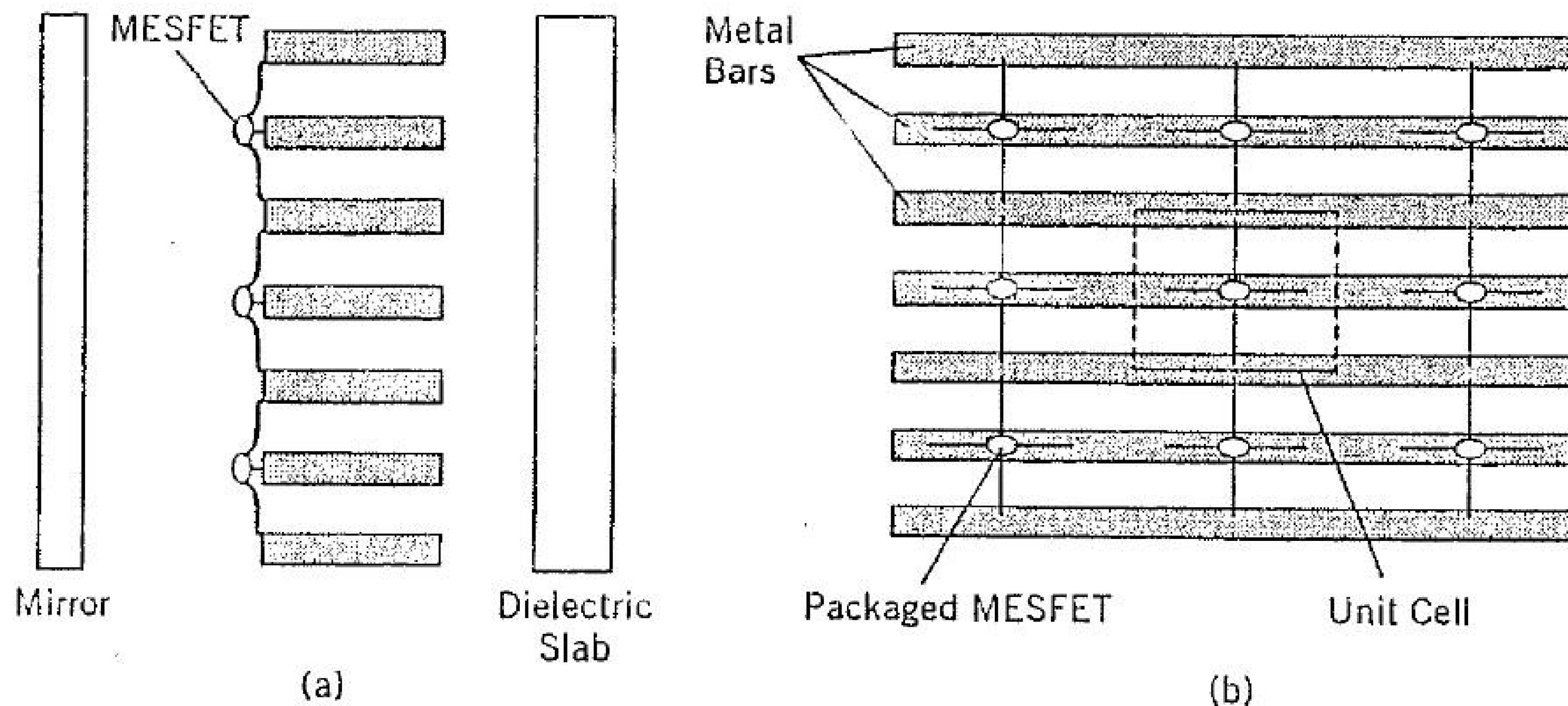


FIGURE 8.7 (a) Side view of the MESFET bar-grid oscillator. (b) Front view of the bar grid. Adjacent rows of devices share bias. The unit cell is shown with solid lines to indicate electric walls and dashed lines to represent magnetic walls.

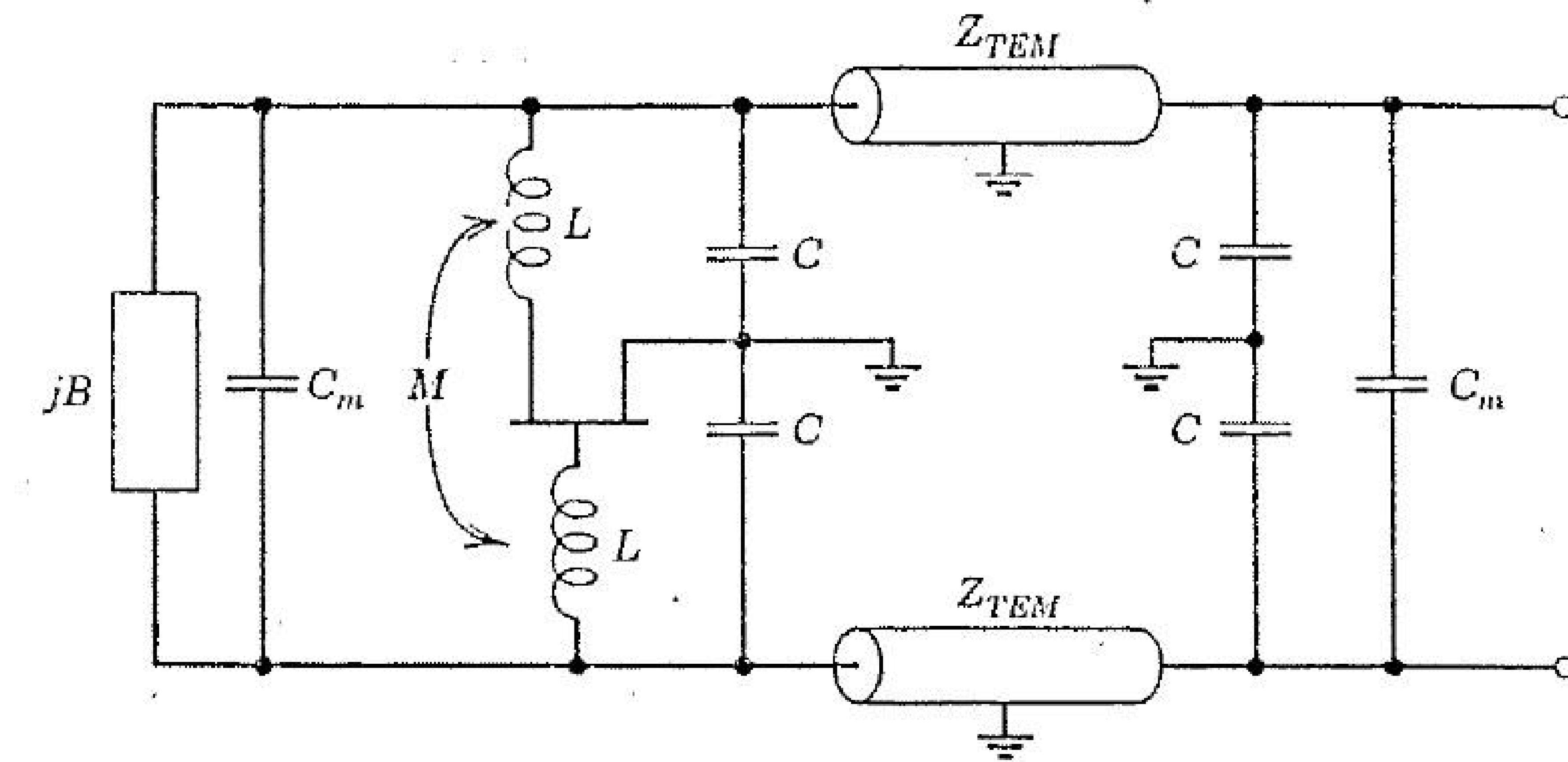


FIGURE 8.8 Transmission line model of the MESFET bar-grid oscillator. The MESFET is added to the model by using its small-signal equivalent circuit.

the metal bars. These waveguides are modeled with two sections of transmission line with characteristic impedance Z_{TEM}. The discontinuity at the edges of the metal bars produces evanescent capacitive modes and is represented with lumped capacitors C and C_m. Here C_m is the mutual capacitance arising from fields of one waveguide coupling to the fields of the other waveguide. Currents on the drain and gate leads generate evanescent inductive modes that we model with lumped inductors. There is also a mutual inductance, M, describing the coupling of the magnetic fields between the metal-bar waveguides.

A grid of 36 MESFETs mounted on metal bars generated 220 mW of power at 3 GHz. The grid period was 10 mm ($0.1\lambda_0$). The measured dc-to-RF conversion efficiency was 22%. Grid directivity, measured from the far-field radiation pattern, was 11.3 dB. Moving the position of the back-short tuned the operating frequency of the grid over a 300-MHz bandwidth. In addition, the frequency could be varied by changing the bias to the gate leads. Gate bias, however, had little effect on the amplitude of the radiated signal, providing a means to frequency-modulate the grid output.

8.3.2 Planar-Grid Oscillators

The transistor grids discussed thus far operate at microwave frequencies. To extend the operating frequencies to the millimeter- and submillimeter-wave region, we need to integrate high-frequency devices into the grid. Packaged devices are unsuitable because of the associated parasitics. In addition, the devices in the grid need to be placed closer together at higher frequencies. Thus, millimeter- and submillimeter-wave grids are only feasible if monolithic fabrication techniques are used. For this reason, planar-grid configurations are particularly important.

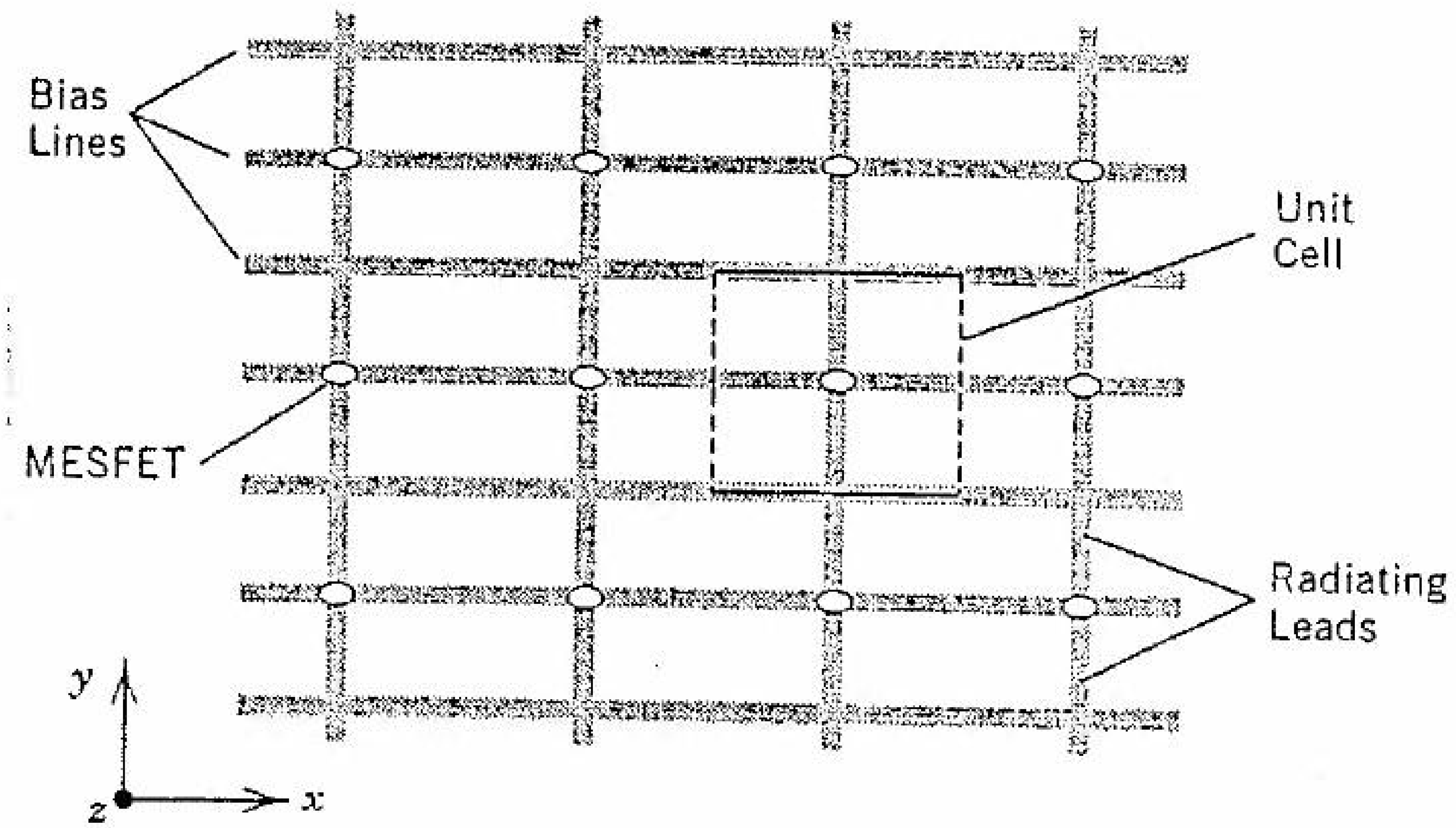


FIGURE 8.9 Physical layout of the planar MESFET grid oscillator. Adjacent rows of devices share bias lines. The unit-cell equivalent waveguide is shown with solid lines for electric walls and dashed lines for magnetic walls.

Several types of planar grids have been investigated [19, 20]. The grids, which have the same basic structure, differ in the manner in which the transistors are connected. A schematic of the planar grid is shown in Figure 8.9. Like the bar grid, vertical leads couple to the radiated field, and horizontal leads are used for dc biasing. Two transistor terminals are connected to the vertical leads, and the third is connected to the horizontal bias line. Initial work with the planar-grid structure utilized packaged MESFETs. Because of the physical layout of the device package, such grids were restricted to the vertical drain-gate configuration illustrated in Figure 8.10(a). More recent grid designs have used chip transistors connected in the vertical drain-source configuration shown in Figure 8.10(b).

To model the behavior of a planar-grid oscillator, we must know what impedances are present at the terminals of a transistor placed in the array. We can define a grid transmission line model (TLM) if we assume that all devices in the grid are identical. For a grid infinite in extent, each transistor will then lie in an equivalent unit cell defined by the grid symmetry. The transmission line model for the grid is shown in Figure 8.11. Terminals 1 and 2 represent connections to the vertical grid leads. The center terminal, 3, represents the horizontal lead. Currents in the vertical leads couple to the radiated field through a center-tapped transformer. Free space is modeled with a 377-Ω resistor scaled by the aspect ratio (b/a) of the unit cell. The mirror behind the grid is represented by a shunt short-circuited stub. The inductance of the radiating leads is shown as a series lumped inductor L. The horizontal leads do not couple directly to the radiated field but do produce evanescent modes that are modeled with a series capacitor and inductor (C_m and L_m). Expressions for the elements in the ECM derived from an EMF

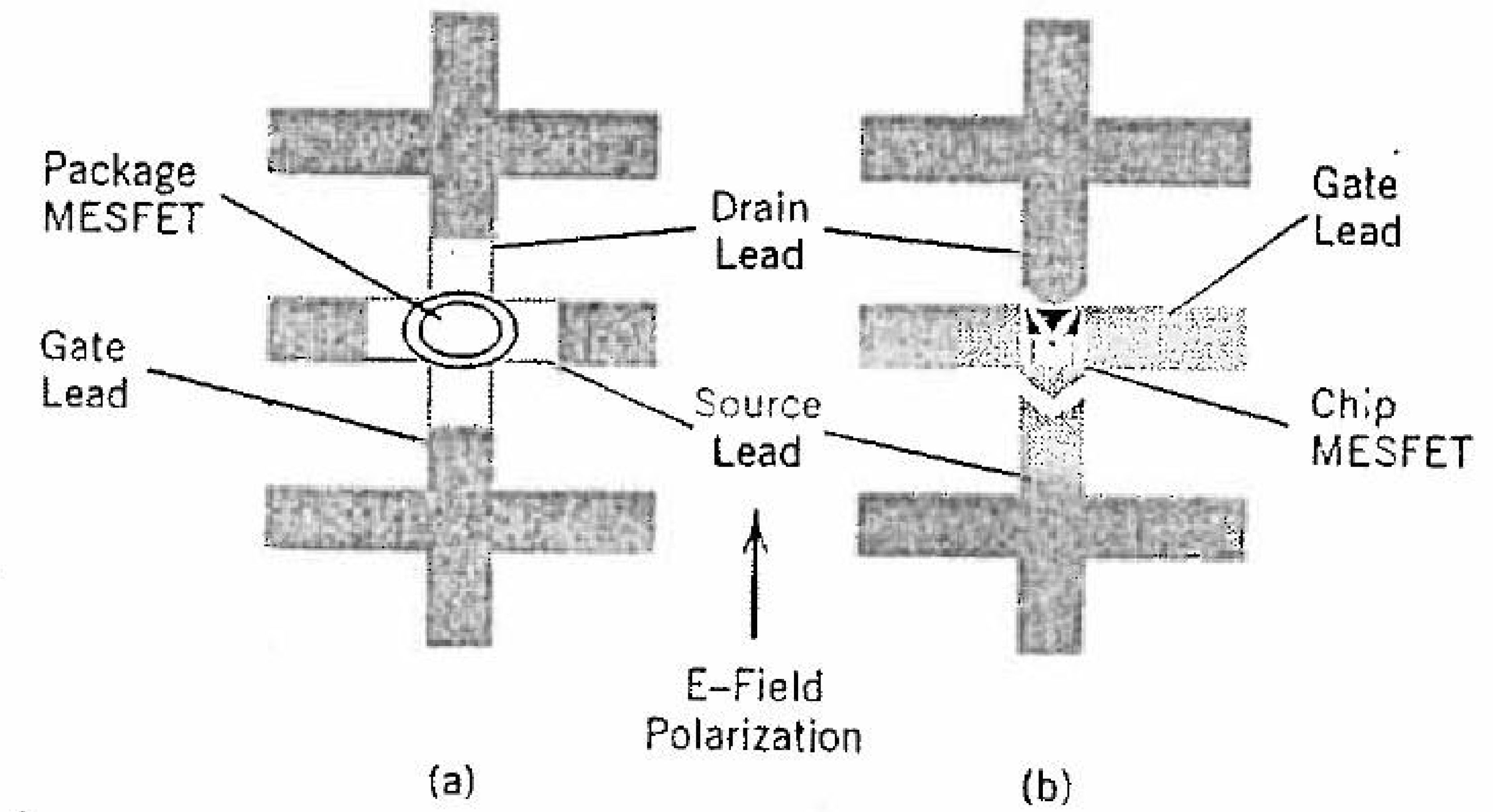


FIGURE 8.10 (a) Unit cell for a vertical drain-gate grid using packaged devices. (b) Unit cell for a gate-feedback grid oscillator with chip transistors. The gate lead, which runs horizontally, is capacitively coupled to the incident electric field.

analysis [12] are

$$L = \frac{2b}{j\omega a} \sum_{\substack{m>0 \\ m \text{ even}}}^{\infty} \operatorname{sinc}^2\left(\frac{m\pi w}{2a}\right) Z_{m0}^{\mathrm{TE}}, \tag{8.5}$$

$$L_m = \frac{4}{j\omega ab} \sum_{\substack{m \text{ even} \\ m,n \neq 0}}^{\infty} \frac{1}{k_c^2} \sin^2\left(\frac{n\pi c}{b}\right) \operatorname{sinc}^2\left(\frac{m\pi w}{2a}\right) \operatorname{sinc}^2\left(\frac{n\pi w_s}{2b}\right) \times \left(\frac{k_x}{k_y} + \frac{k_y a}{k_x(a-w)}\right)^2 Z_{mn}^{\mathrm{TE}}, \tag{8.6}$$

$$\frac{1}{C_m} = j\frac{2\omega}{ab}\left(\sum_{n=1}^{\infty} \frac{1}{k_y^2} \sin^2\left(\frac{n\pi c}{b}\right) \operatorname{sinc}^2\left(\frac{n\pi w_s}{2b}\right) Z_{0n}^{\mathrm{TM}} + 2\sum_{\substack{m \text{ even} \\ m,n \neq 0}}^{\infty} \frac{1}{k_c^2} \sin^2\left(\frac{n\pi c}{b}\right) \operatorname{sinc}^2\left(\frac{n\pi w_s}{2b}\right) \operatorname{sinc}^2\left(\frac{m\pi w}{2a}\right)\left(1 - \frac{a}{a-w}\right)^2 Z_{mn}^{\mathrm{TM}}\right). \tag{8.7}$$

In these expressions $k_x = m\pi/a$, $k_y = n\pi/b$, and $k_c^2 = k_x^2 + k_y^2$, where m and n are integers; Z_{mn}^{TE} and Z_{mn}^{TM} are the wave impedances for the mnth TE and TM modes [13]. Each of these is a parallel combination of the impedances in the $+z$ and $-z$ directions.

The TLM for the grid is completed by adding the ECM for the transistor. For the complete circuit representing the vertical drain-source configuration

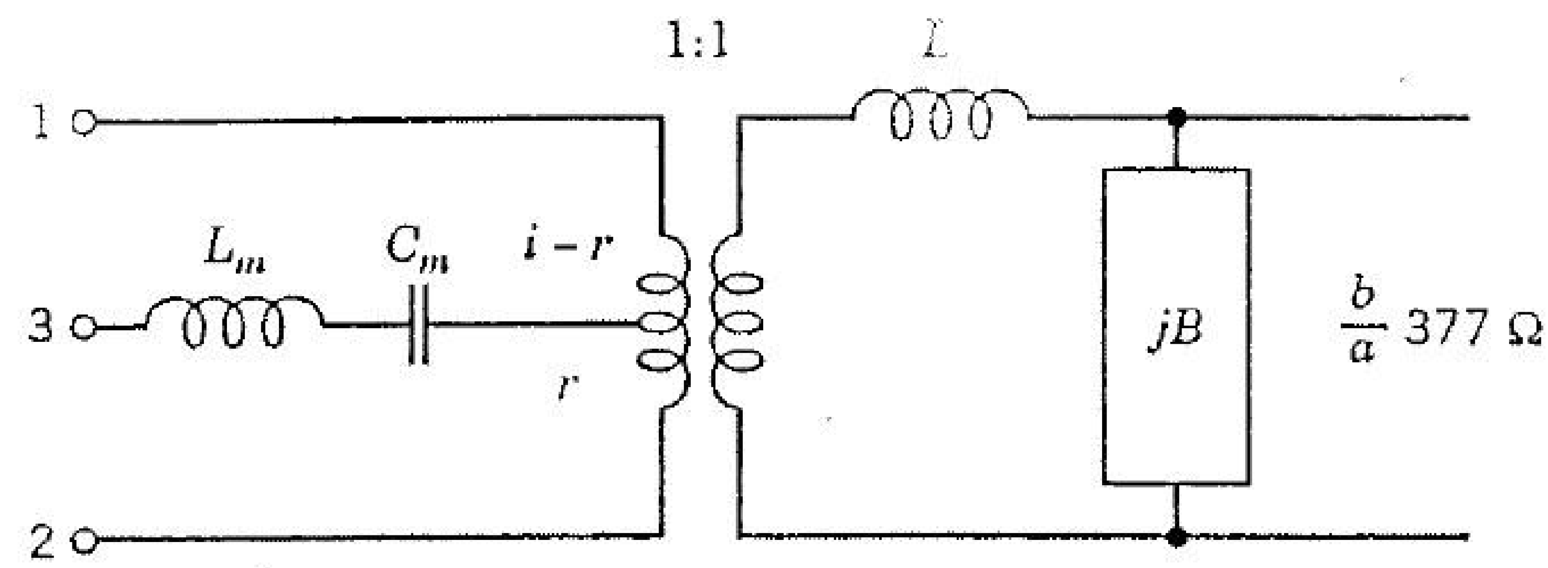


FIGURE 8.11 Transmission line model for the planar MESFET grid. The transformer turns ratio is defined as $r = c/b$.

of Figure 8.10(b) the drain and source of the transistor are connected to TLM terminals 1 and 2. Because the grid embedding network provides a feedback path between the drain and gate, we refer to the vertical drain-source configuration as a "gate-feedback" grid. The transconductance current of the transistor is controlled by the voltage appearing across the gate-source capacitor. The loop gain of the circuit can be calculated by using a conventional microwave circuit design package to predict the oscillation frequency.

The design of a planar-grid oscillator begins with the choice of the active device, substrate, and oscillation frequency. To date, the best results have been obtained on low-dielectric substrates, such as Duroid 5880 with a dielectric constant $\epsilon_r = 2.2$. Experience has shown that it is desirable to keep the grid unit cell as small as possible to avoid the generation of undesirable substrate modes. If λ_d is the wavelength in the dielectric, then for unit cells larger than λ_d, substrate modes will begin to propagate. It should be reasonable to build grids as large as $\frac{2}{3}\lambda_d$; however, grids only up to $\lambda_d/2$ have been tested. Based on the mentioned constraints, the size of the unit cell is chosen and values for the grid elements computed. At this stage of the design, it is generally most efficient to use the EMF method equations (8.5–8.7) to compute the element values. Appendix A lists a C++ program for computing the EMF-derived S-parameters of the grid elements over the frequency range of interest. Even with a modest 386-based personal computer, S-parameters will be generated in a few seconds per frequency point.

The grid-element S-parameters can then be inserted into the ECM for the grid and the approximate oscillation frequency computed using traditional linear oscillator circuit analysis. If the analysis shows the grid will not oscillate, or is not oscillating at the desired frequency, for any reasonable mirror position, then the grid unit-cell size, lead dimensions, and substrate thickness can be adjusted in an iterative fashion until the loop gain has a magnitude greater than unity and 0° phase at the desired oscillation frequency. Typically, a commercial linear microwave design package would be used for the simulations. The fast computation of the grid-element S-parameters using the EMF solution allows many iterations of the design cycle to be performed in a very short time.

A design based on the EMF method alone is likely to have an uncertainty in oscillation frequency up to 10% based on experimental results to date. For this reason it may be desirable to simulate the grid unit cell designed by the EMF method with a potentially more accurate technique, such as a commercial finite-element electromagnetic solver, or a MOM analysis to further fine-tune the design before fabrication. This is particularly important if the grid metallization pattern differs significantly from the simple crossed-dipole solution presented here.

Strictly speaking, a TLM derived using an equivalent waveguide is valid only for infinite grids. Hence, the applicability of the model is questionable with small grids because the equivalent waveguide boundary conditions do not hold at the grid edges. It may be possible, however, to terminate the grid edges in a way that simulates the equivalent waveguide boundary conditions. Electric walls at the top and bottom of the grid can be approximated with vertical $\lambda/4$ open-circuited stubs. This should prevent currents there from abruptly dropping to zero. In addition, RF chokes or inductive leads can be used at the sides of the grid to create large impedances, thus simulating magnetic walls. One particularly effective approach is to use ferrite slabs glued to the vertical edges of the grid. Using edge terminations such as these, the EMF models have shown reasonably good agreement with measurement for grids containing as few as 16 elements.

Grid oscillators based on the vertical drain-gate configuration of Figure 8.10(a) are called "source-feedback" grids. This terminology arises because the vertical leads (drain and gate) couple directly to the radiated field and part of this radiated field is capacitively coupled to the horizontal transistor lead (the source) through the grid embedding circuit. A 100-element grid based on the unit cell of Figure 8.10(a) was built on a multilayer dielectric substrate. Devices in the grid were spaced 8 mm apart. The grid, which oscillated at 5 GHz, produced 550 mW of power with a dc-to-RF efficiency of 20%. A planar mirror behind the grid was used to tune the frequency and output power [19].

A disadvantage of the common-source grid is the radiating gate lead. Because the gate strongly couples to the radiated field, the grid tends to oscillate at lower frequencies where the devices have high gain. The common-gate grid of Figure 8.10(b) does not exhibit this problem because the gate is connected to the horizontal lead. This allows the feedback between the radiated field and the gate to occur through the grid embedding circuit. Figure 8.12 shows a 16-element gate-feedback grid designed for operation in the X band. Chip MESFETs, spaced 9 mm apart, were soldered and wire-bonded to the grid. The grid oscillated at 11.6 GHz and produced 335 mW of output power, corresponding to a dc-to-RF efficiency of 20% [20].

Illustrating that planar grids can be scaled for use at higher frequencies, this X-band gate-feedback grid was redesigned for operation in the Ku band.

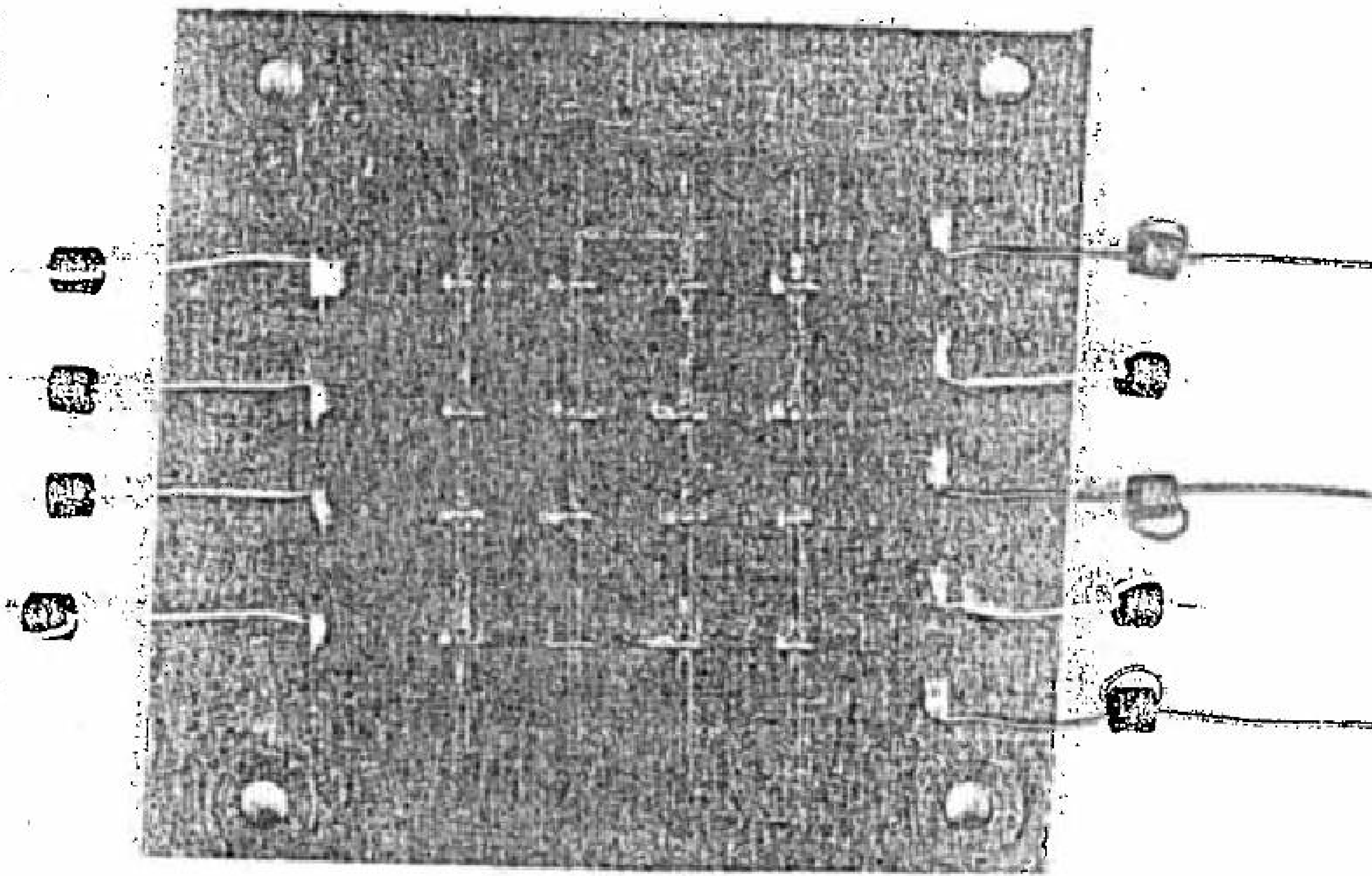


FIGURE 8.12 An X-band planar-grid oscillator. The grid is placed between a mirror and dielectric slab that form the Fabry-Perot cavity. Ferrite beads are placed on the bias lines to suppress low-frequency oscillations.

With an identical substrate and the same devices, a scaled 36-element grid produced 235 mW at 17 GHz. This oscillation frequency is near the f_T of the transistors (19 GHz), suggesting that suitably designed transistor grids may oscillate well over 100 GHz.

8.3.3 Power-Grid Oscillators

To demonstrate watt-level powers from a quasi-optical grid oscillator, existing power oscillator design principles must be integrated with quasi-optical grid oscillator theory. Factors to consider when designing for maximum power include device characteristics, device load impedance and feedback loop gain optimization, heat dissipation, device biasing, and grid edge effects.

The high powers dissipated by power transistors and the high device densities achieved with quasi-optical grid techniques mean that careful thermal design of the grid is required if the device temperatures are to remain within safe limits (typ. < 150°C). There are basically two paths for the removal of heat from devices loaded in a grid. The heat can be extracted by conduction through the substrate to the grid edges, or the heat can be extracted by convection and radiation to the ambient medium surrounding the grid.

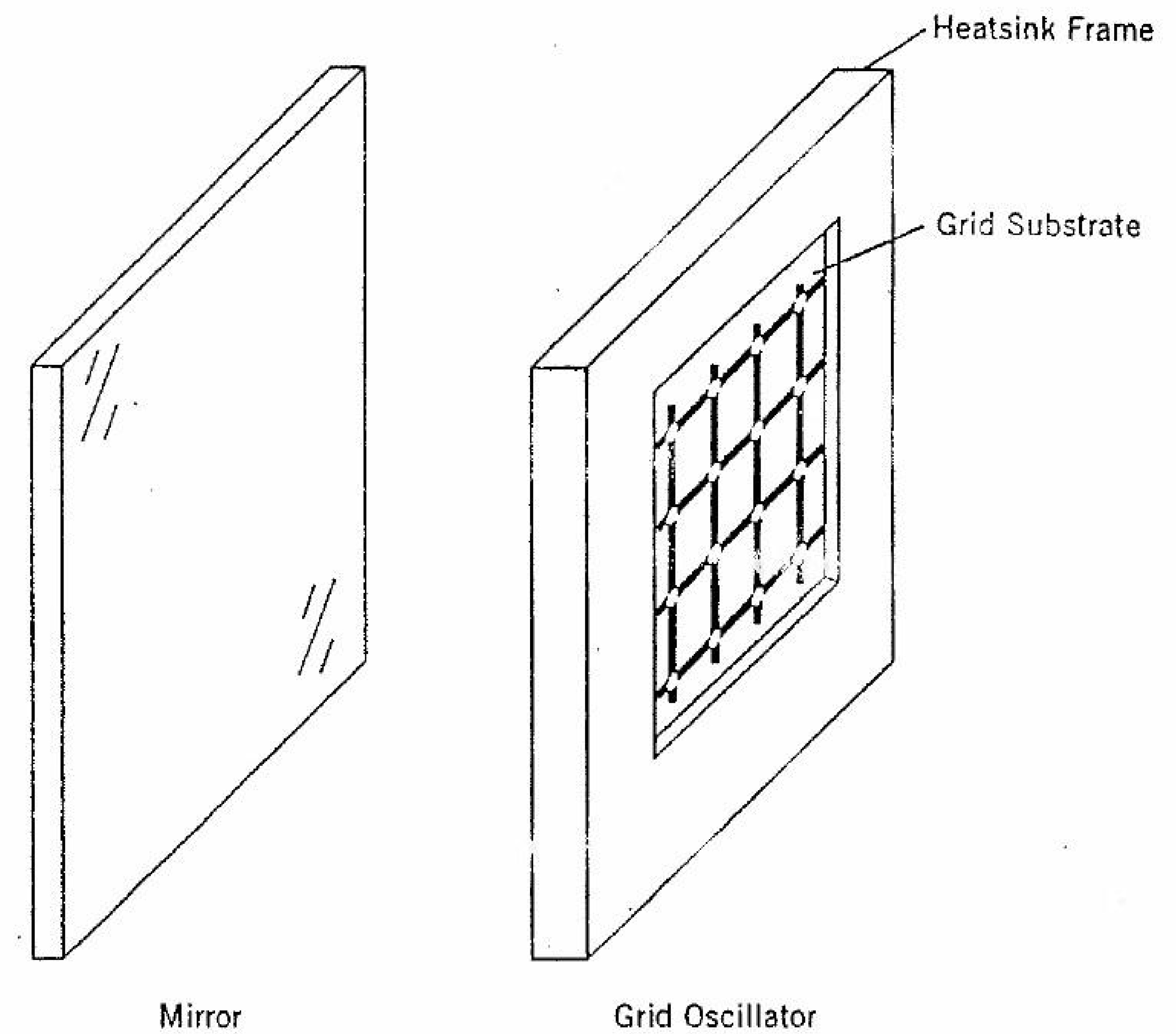


FIGURE 8.13 Grid cooling by thermal conduction through the substrate to a frame held at constant temperature.

To model a grid cooled by substrate conduction, we can compute the thermal resistance by conduction through a substrate for a square grid with uniform heat flux entering from the top and grid edges maintained at a constant temperature. This would simulate the case of a grid mounted on a heatsink frame as shown in Figure 8.13. The analysis essentially solves Laplace's equation,

$$\nabla^2 T = 0, \tag{8.8}$$

with boundary conditions $T = T_{\text{sink}}$ at the grid edges, $\psi = \text{const}$ for the top face, and $\psi = 0$ for the bottom face; T is the grid temperature, T_{sink} is the heatsink temperature, a constant, and ψ is the heat flux density at the grid surface. Based on this type of analysis, the temperature will reach a peak at the center of the grid where the devices are furthest from the heatsink. Figure 8.14 shows the expected temperature profile for a grid of transistors mounted on a 75-mm square that is 1.6 mm thick. The peak transistor channel temperature at the center of the grid is

$$T_{\text{ch}} = P_d(R_{\text{th}} + R_{\text{gh}}), \tag{8.9}$$

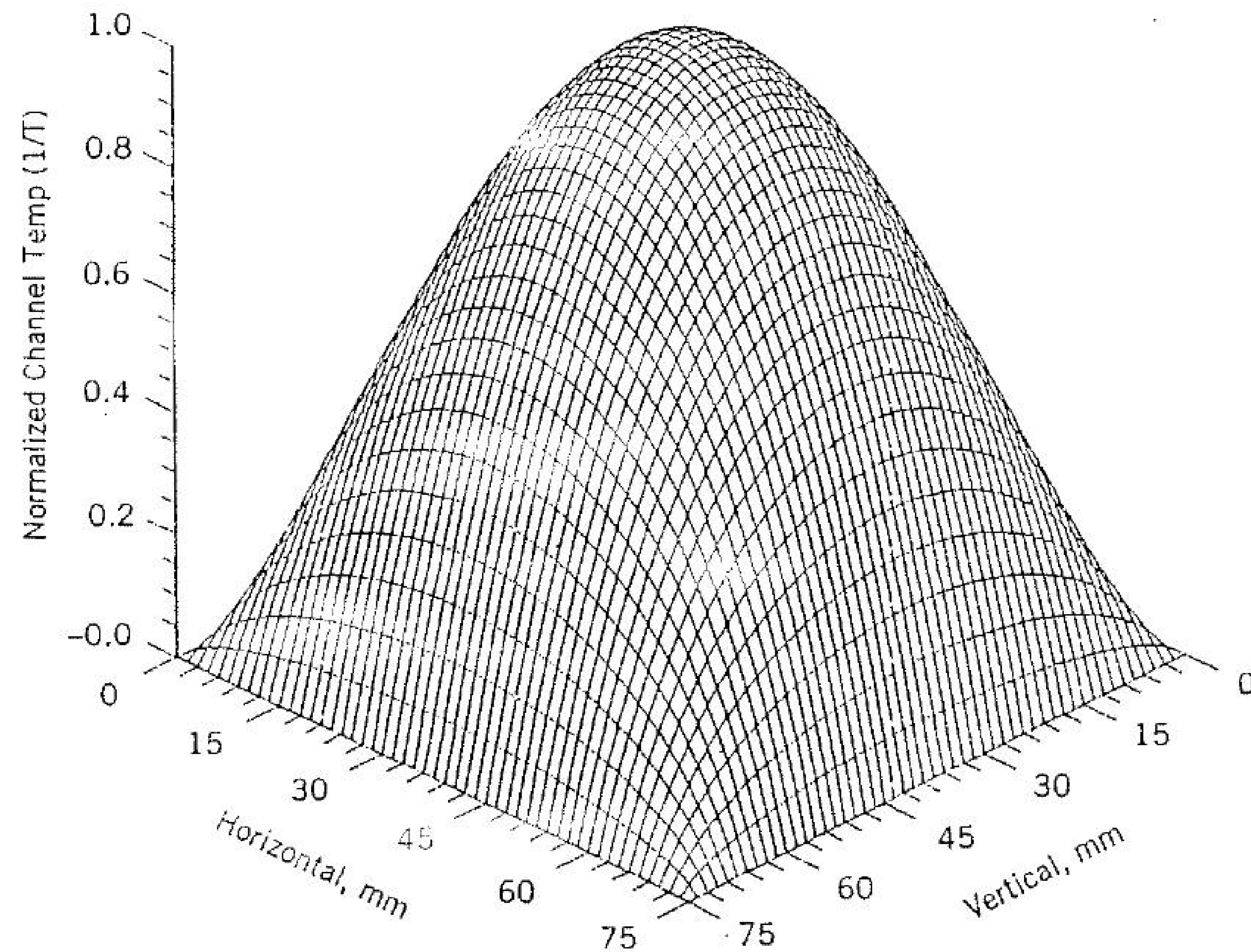


FIGURE 8.14 Normalized transistor channel temperature profile for a uniform grid of transistors. The grid is assumed to be 75 mm square and 1.6 mm thick.

where T_{ch} is the transistor channel temperature, P_d is the device power dissipation, R_{th} is the transistor channel-to-case thermal resistance, and R_{gh} is the equivalent grid thermal resistance at the center given approximately by

$$R_{gh} = n\left(\frac{0.29}{ka}\right)\left[1 + \left(\frac{0.254a}{t}\right)^{2.55}\right]^{1/2.55}, \tag{8.10}$$

where a is the grid length, t is the substrate thickness, n is the number of devices in the grid, and k is the substrate thermal conductivity. It is clear that for conduction cooling to be effective, a grid substrate with a high thermal conductivity is required. Typical substrates suitable for conduction cooling are diamond and aluminum nitride.

Modeling heat flow by convection is much more difficult than the conduction case described before. Simple models to describe convection are not available, and most published work is empirical in nature. Consequently, it is easier to characterize the grid thermal resistance due to convection by the use of infrared thermal mapping measurements of a grid fabricated out of the desired substrate with resistors in place of the devices. Based on the power dissipated by the resistors, it is then possible to compute the thermal

resistance of the grid. This thermal resistance, along with the device case-to-channel thermal resistance, can then be used to predict the channel temperatures for the high-power transistors.

To get the most power out of the transistors, we must design the grid to provide an optimal impedance across the transistor output terminals. Ideally, a nonlinear model for the device would be used to simulate the saturated transistor in the grid circuit. Alternatively, approximations can be made that allow linear design tools to be substituted with reasonable accuracy. One such approximation is based on a simple load-line analysis described by Cripps [21, 22]. This simple theory can be used to compute the approximate optimal load impedance to present to the transistor for maximum power. This method has been employed successfully for years in the design of power amplifiers.

The optimal load is defined as the impedance that allows the device output terminals to swing between the maximum allowable voltage and current limits. For a MESFET this optimal load resistance R_{opt} is approximated by

$$R_{opt} = \frac{2V_{dc}}{I_{DSS}}, \tag{8.11}$$

where V_{dc} is the drain-source dc bias voltage and I_{DSS} is the maximum saturated drain current. This resistance is presented to the current source terminals of the transistor equivalent circuit as shown in Figure 8.15.

Although defining the approximate optimal load resistance R_{opt} is relatively simple, designing a grid oscillator to present that impedance to the transistor is quite challenging. One approach is to reduce the grid oscillator to an equivalent circuit by using one of the techniques described earlier. The transistor model is then connected to this circuit, and the internal loop gain of the oscillator is computed by linear analysis. The grid dimensions are adjusted until the loop gain has a magnitude greater than unity and 0° phase at the desired oscillation frequency. Typically, a commercial linear microwave design package would be used for the simulations. By varying substrate thickness, the grid pattern, unit-cell size, and the mirror separation behind the grid, one can usually obtain a circuit that oscillates at the desired frequency and provides the desired load impedance to the transistor.

For maximum oscillator power, Johnson has shown that the transistor must be operating at the point where maximum power-added efficiency occurs [23]. Since this is a function of gain compression, or transistor saturation, it can be controlled by varying the amount of feedback applied to the transistor. Too little feedback will result in too little saturation of the transistor, resulting in low output power. Too much feedback will cause too much power to be fed back to the transistor, decreasing available output power as well as potentially damaging the devices.

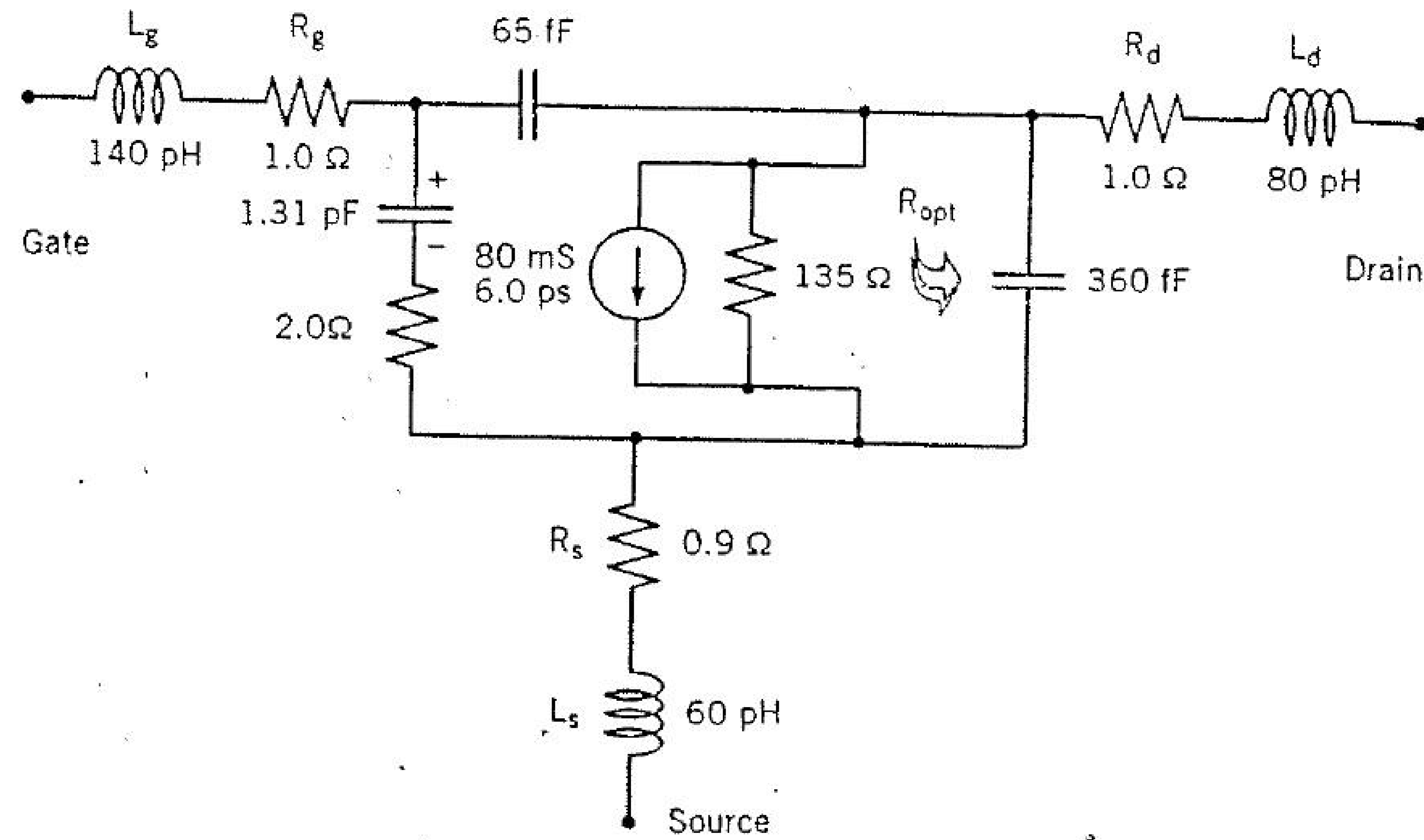


FIGURE 8.15 Linear lumped-element model for a typical power MESFET. The approximate optimal load impedance, R_{opt}, calculated using (8.11), is presented across the terminals of the internal current source of the MESFET model.

The oscillator output power P_{osc} is

$$P_{osc} = P_{out} - P_{in}, \tag{8.12}$$

where P_{out} is the output power of the transistor, and P_{in} is the power fed back to the transistor input. Since P_{out} cannot increase above the saturated power of the transistor, a plot of P_{osc} versus P_{in} shows a maximum value for some intermediate value of P_{in} (Figure 8.16).

The maximally efficient power gain G_{ME} is defined by Kotzebue [24] as the power gain that maximizes the two-port added power for a given input power—that is, the gain that maximizes $(P_{out} - P_{in})/P_{in}$ and can be computed from the relation

$$G_{ME} = \frac{|s_{21}/s_{12}|^2 - 1}{2[K|s_{21}/s_{12}| - 1]}, \tag{8.13}$$

where K, Rollett stability factor, is

$$K = \frac{1 + |s_{11}s_{22} - s_{21}s_{12}|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{12}||s_{21}|}. \tag{8.14}$$

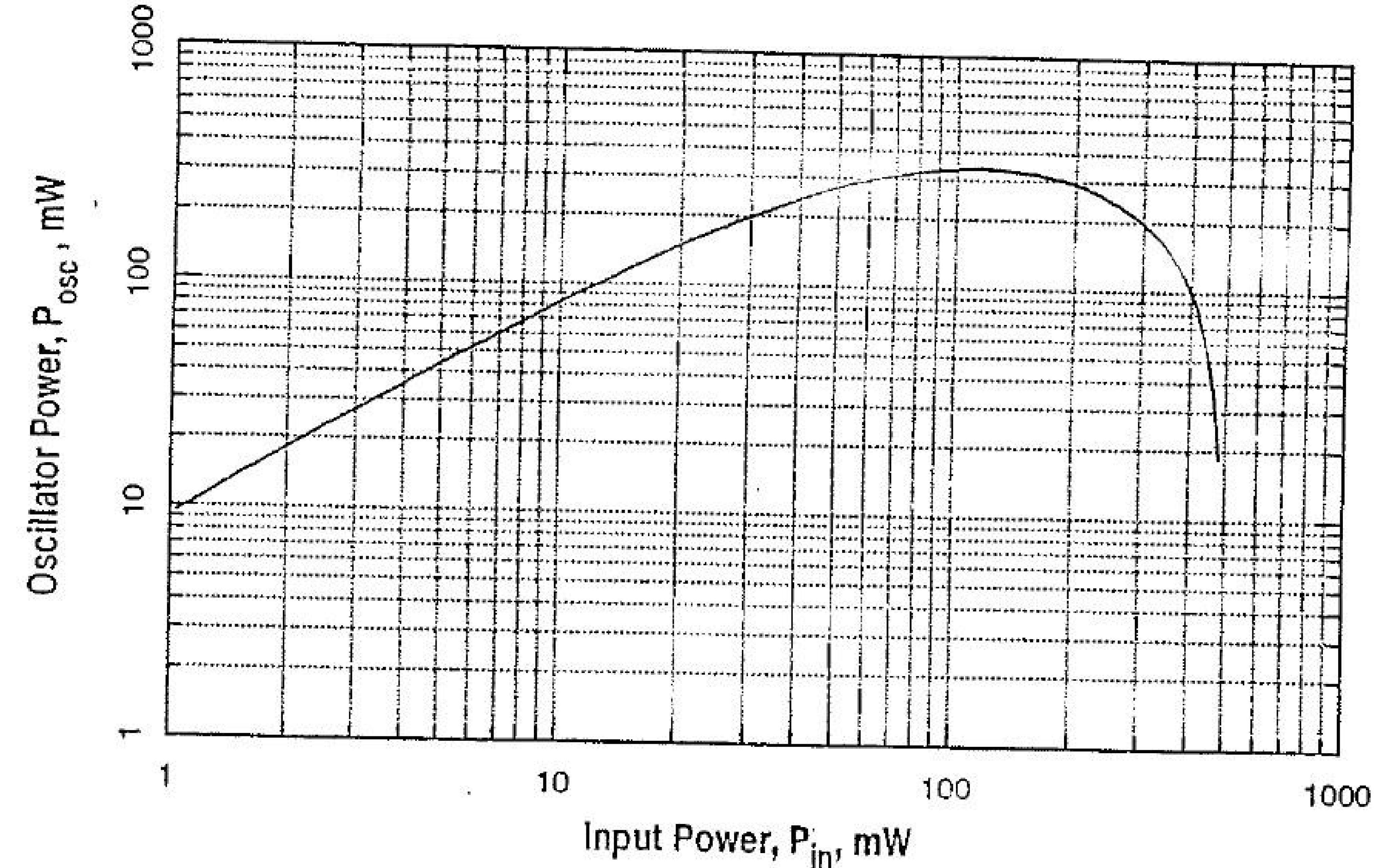


FIGURE 8.16 A plot of oscillator output power, P_{osc}, vs. input power, P_{in}, for a Fujitsu FLK052XP power MESFET at 10 GHz. The peak power of 330 mW occurs at 4 dB of gain compression.

We can approximate the power saturation curve of a MESFET, using the following exponential fit:

$$P_{out} \simeq P_{sat}\left[1 - e^{-G_{MEss}P_{in}/P_{sat}}\right], \tag{8.15}$$

where P_{sat} is the maximum saturated power of the transistor and G_{MEss} is the small-signal maximally efficient gain computed by using the transistor small-signal S-parameters and Eq. (8.13). We solve for maximum oscillator power by maximizing $P_{out} - P_{in}$—that is by solving $\partial P_{out}/\partial P_{in} = 1$, which gives

$$P_{osc}(\max) = P_{sat}\left[1 - \frac{1}{G_{MEss}} - \frac{\ln G_{MEss}}{G_{MEss}}\right]. \tag{8.16}$$

The corresponding maximally efficient gain that gives maximum oscillator power, G_{MEsat}, is then

$$G_{MEsat} = \frac{G_{MEss} - 1}{\ln G_{MEss}}. \tag{8.17}$$

The required level of saturation can then be determined by the simple

formula

$$\mathrm{SAT} = G_{\mathrm{MEss}} - G_{\mathrm{MEsat}}. \tag{8.18}$$

The first grid oscillators investigated used unit cells that provide a feedback path that is largely internal to the grid. This intragrid feedback is difficult to control with any precision by varying the usual physical grid parameters such as unit-cell size and lead widths. The resulting feedback also tends to be much larger than is desirable from the standpoint of maximum oscillator output power.

An examination of the equivalent circuit for the crossed-dipole grid used with good success in the past for grid oscillators (Figure 8.11) shows that the components that most directly affect feedback are the center-tapped inductor, L_m, and capacitor, C_m, of the grid equivalent circuit. The values of these components are complicated functions of many variables that describe the unit-cell geometry. It is not generally possible to adjust these components individually without affecting the values of everything else in the equivalent circuit. However, it is possible to gain some control over these components by altering the shape and position of the horizontal strip that connects to the gate of the transistor. Figure 8.17 shows the basic idea. To increase the inductance L_m, we can *meander* the center lead as shown in Figure 8.17(a). This will decrease the internal feedback loop gain. To vary the capacitive coupling to the center lead, we can bend the center lead into a V-shape as shown in Figure 8.17(b). If the strip is bent closer to the vertical strip connected to the transistor's drain, drain-gate coupling, and hence feedback loop gain, should increase. Conversely, if the strip is bent closer to the vertical strip attached to the transistor's source, drain-gate coupling should decrease.

Of these two schemes the meandered center lead is the easiest to implement because the same equivalent circuit can be used that was found for the original crossed-dipole unit-cell EMF analysis in Figure 8.11. The meandered lead should primarily affect the value of L_m in the ECM. The new value of L_m can be computed by using a finite-element electromagnetic engine to solve for the S-parameters of the meandered unit cell and then parameter-fitting the model to the simulated results.

Using a meandered horizontal strip is not a completely independent method of controlling feedback loop gain because it also affects the oscillation frequency and transistor load impedance. However, simulations have shown that varying the device offset within the unit cell and increasing the gate lead inductance allows the feedback to be reduced while preserving the desired transistor drain-source load impedance. Empirically, it has been observed that increasing the gate lead inductance lowers the loop gain but also lowers the real impedance and increases the inductive reactance presented to the transistor drain-source terminals. It also tends to shrink the unit-cell size for a given oscillation frequency. The increase in inductive

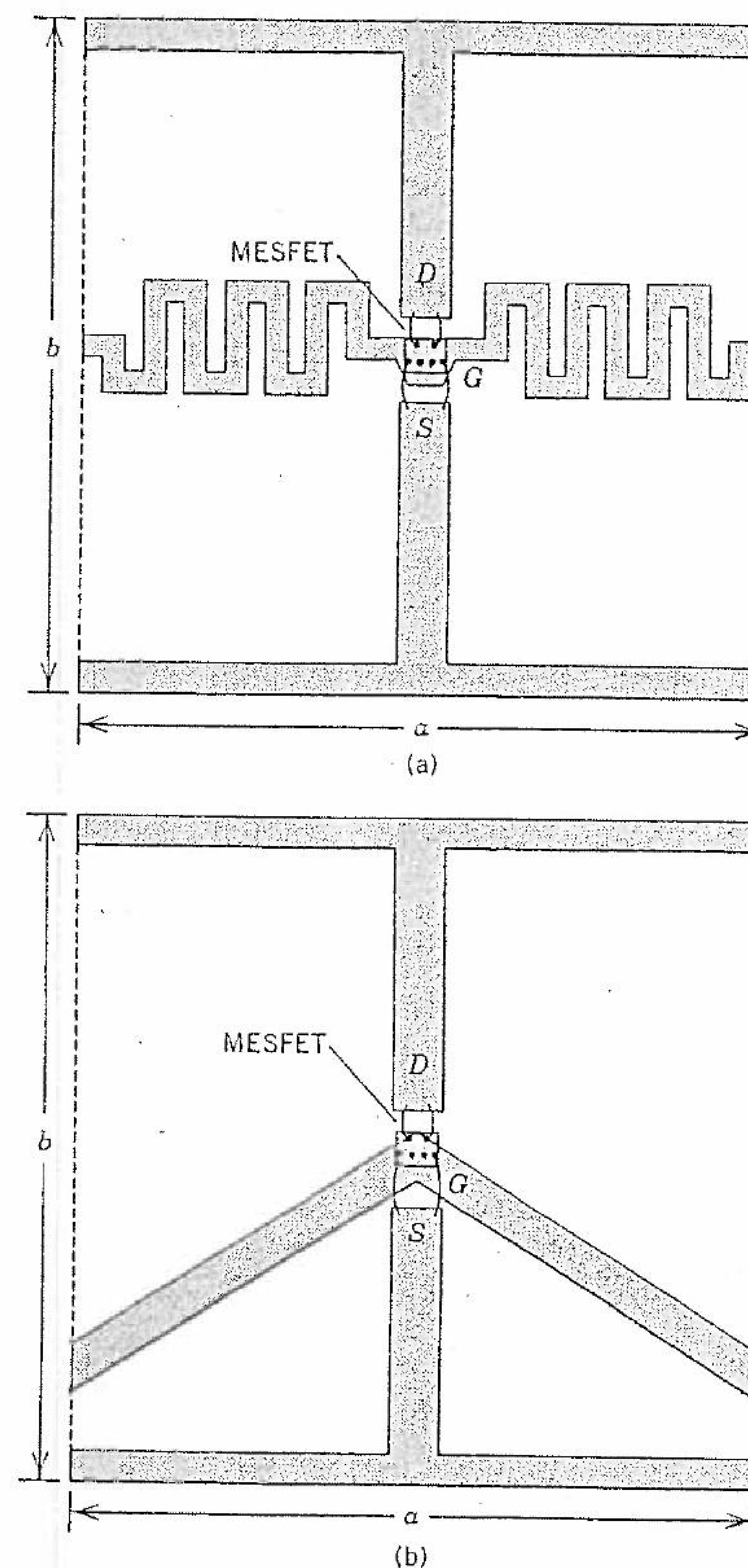


FIGURE 8.17 Controlling intragrid feedback loop gain. (a) Meandering the horizontal strip connected to the transistor's gate can be used to increase the value of L_m. (b) Bending the horizontal strip toward or away from the vertical strip connected to the transistor's drain lead varies the drain-gate coupling.

reactance can be compensated by offsetting the transistor position in the unit cell so that the drain-lead length is shortened. Fine tuning of the mirror position can then be used to find the point where the loop gain and real resistance presented to the transistor are as close as possible to the desired values.

Following these design techniques, a high-power X-band 100-transistor grid oscillator has been demonstrated based on commercial MESFET power transistors [25]. The grid embedding circuit was designed to provide the optimal load impedance and feedback loop gain to the transistor for maximum power. The measured ERP was 660 W and the directivity was 18.0 dB. This corresponds to a total radiated power of 10.3 W, or 103 mW per device, resulting in an overall dc-to-RF efficiency of 23%.

8.4 GRID MIXERS

A grid loaded with diodes produces a nonlinear device suitable for mixing or detecting quasi-optical signals with improved dynamic range compared to conventional single-diode mixers. Few other circuit topologies exist that address the problems of intermodulation distortion and dynamic range in high-frequency mixers. In addition, the quasi-optical grid mixer is ideally suited for photolithographic fabrication, making it an excellent candidate for monolithic integration on high-performance semiconductor substrates. Such a monolithic grid mixer potentially allows significant improvements in power handling and dynamic range for mixers operating in the millimeter-wave band and above.

A planar-grid mixer is shown in Figure 8.18. Diodes are loaded periodically in the grid, each diode defining a unit cell of the grid. A flat metal mirror behind the grid acts as a reactive tuning element. The grid mixer reflection coefficient is optimized for incident signals at the design frequency by optimizing the dimensions and metal pattern of the unit cell and the electrical properties of the grid substrate. Diodes in each column are connected in series. The intermediate-frequency (IF) voltages add along each column and are collected at the diode terminals forming the top and bottom edges of the grid. A dc bias may also be applied at the grid edges. The symmetry of the grid cancels any RF currents along the horizontal rows.

Each diode in the array is presented with an embedding impedance that is a function of the grid structure repeated throughout each unit cell. Two grid designs that work well are the dipole (Figure 8.19(a)), consisting of a vertical strip running down the center of the grid unit cell with the diode bridged across a gap in the strip, and the bow tie (Figure 8.19(b)), with the diode located at the apex of the bow tie.

To understand how the grid mixer improves signal power handling and dynamic range, we first need to investigate the noise performance of a grid of diodes. One might expect that the noise power of the grid mixer is the same

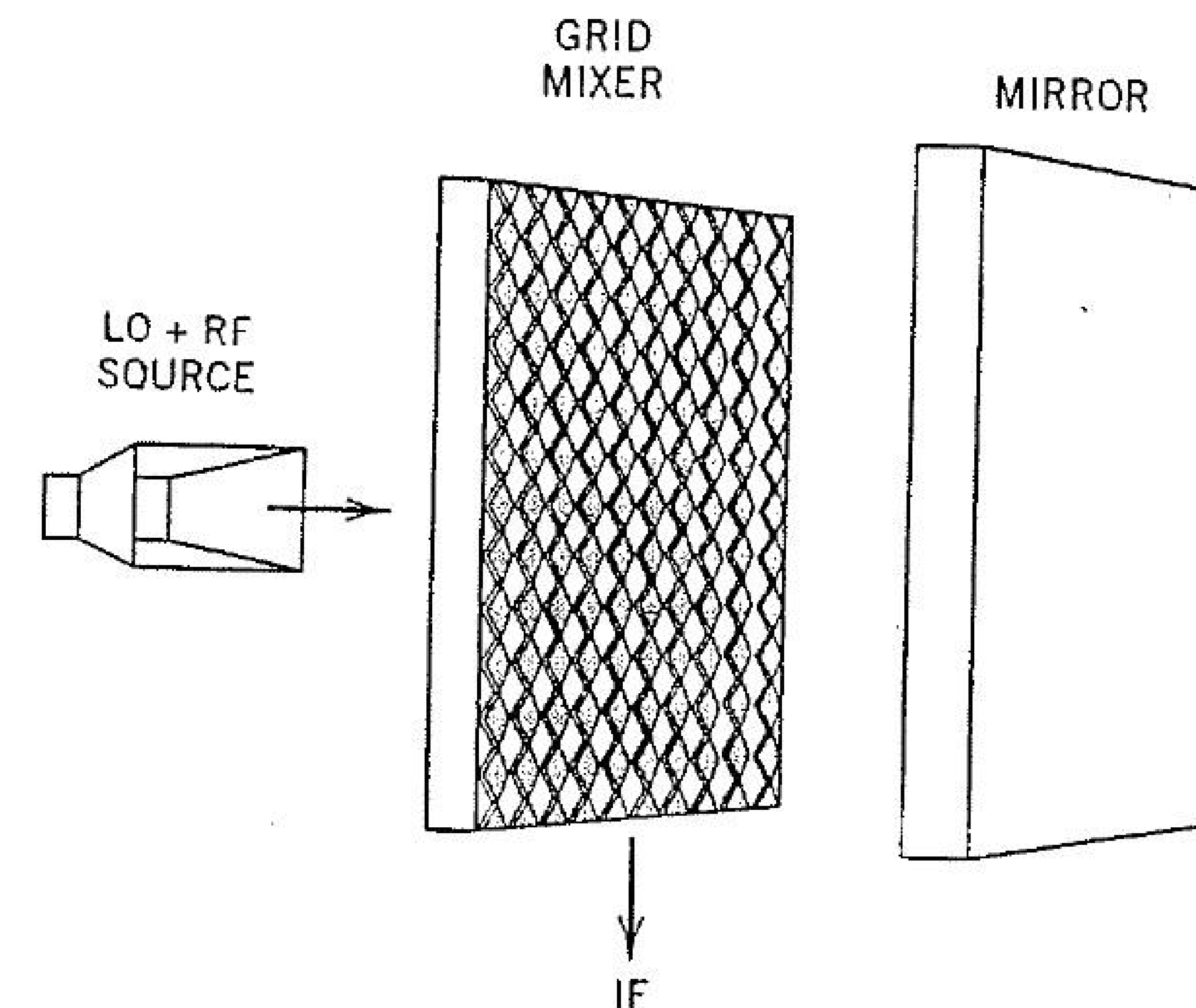


FIGURE 8.18 The grid mixer. The RF and LO signals couple to the diodes quasi-optically through the face of the grid. The IF signal is generated across the top and bottom grid edges. The mirror is used to tune out the capacitive reactance of the diodes for a better match to free space.

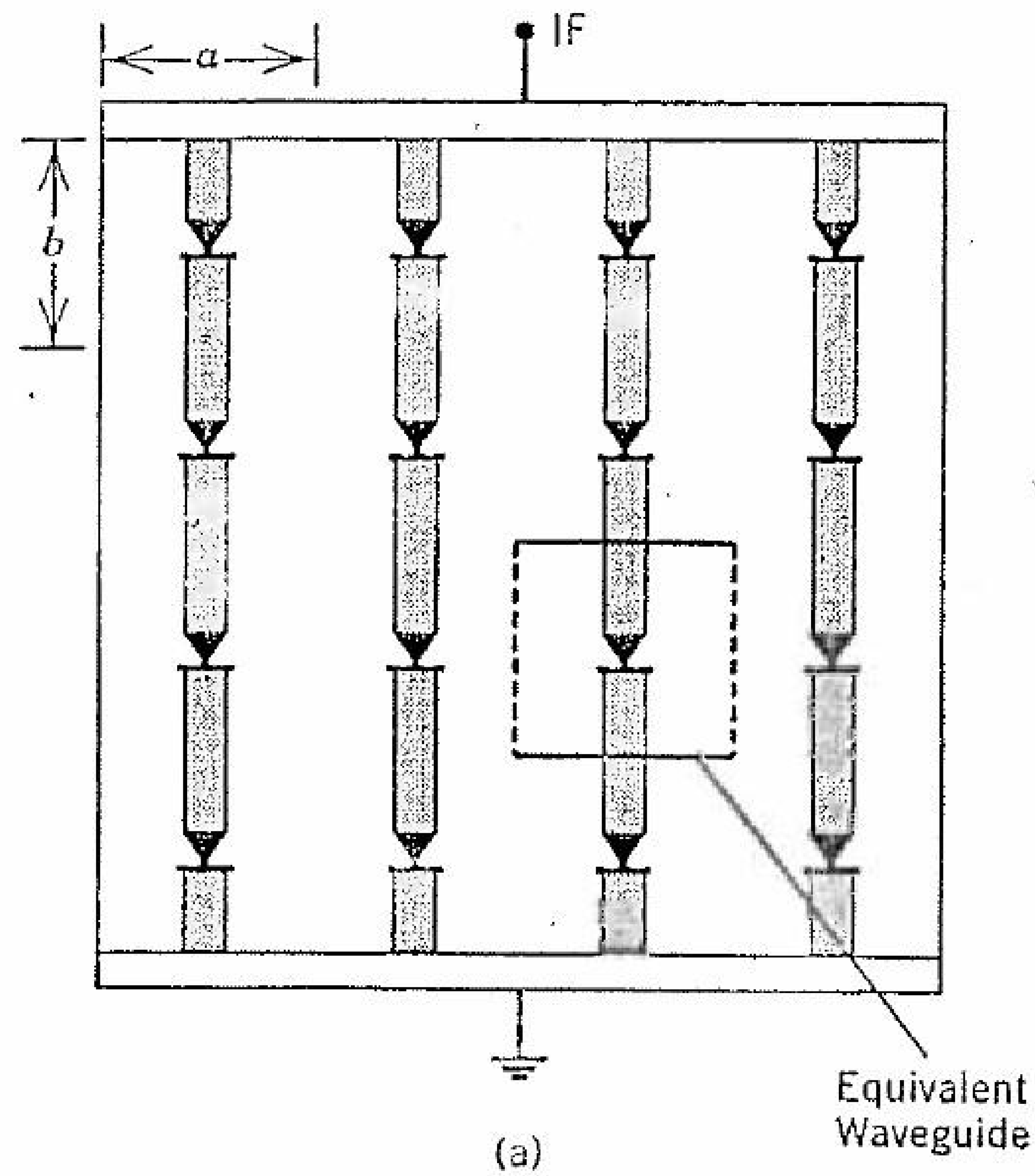
as the noise power of a single-diode mixer because the individual noise powers from each diode are uncorrelated. Consequently, the noise figure of the grid mixer will be the same as an equivalent single-diode mixer. This can be shown mathematically if we look at the equivalent circuit of a single diode shown in Figure 8.20(a). A single diode can be represented as a Thevenin equivalent circuit with a source resistance R_d in series with an rms noise voltage ΔV_d and an rms IF signal voltage V_d^{IF} so that

$$P_d^{\mathrm{IF}} = \frac{P_d^{\mathrm{RF}}}{L_C} \tag{8.19}$$

and

$$P_d^{\mathrm{IF}} = \frac{(V_d^{\mathrm{IF}})^2}{R_d}, \tag{8.20}$$

where L_C is the RF-to-IF conversion factor of the diode, a function of the LO power, P_d^{IF} is the converted IF signal power, and P_d^{RF} is the RF signal power absorbed by the diode. If the diodes are connected in a rectangular grid with m rows and n columns, there will be m diodes in series per column and n diodes in parallel per row. Consequently, we can define a Thevenin



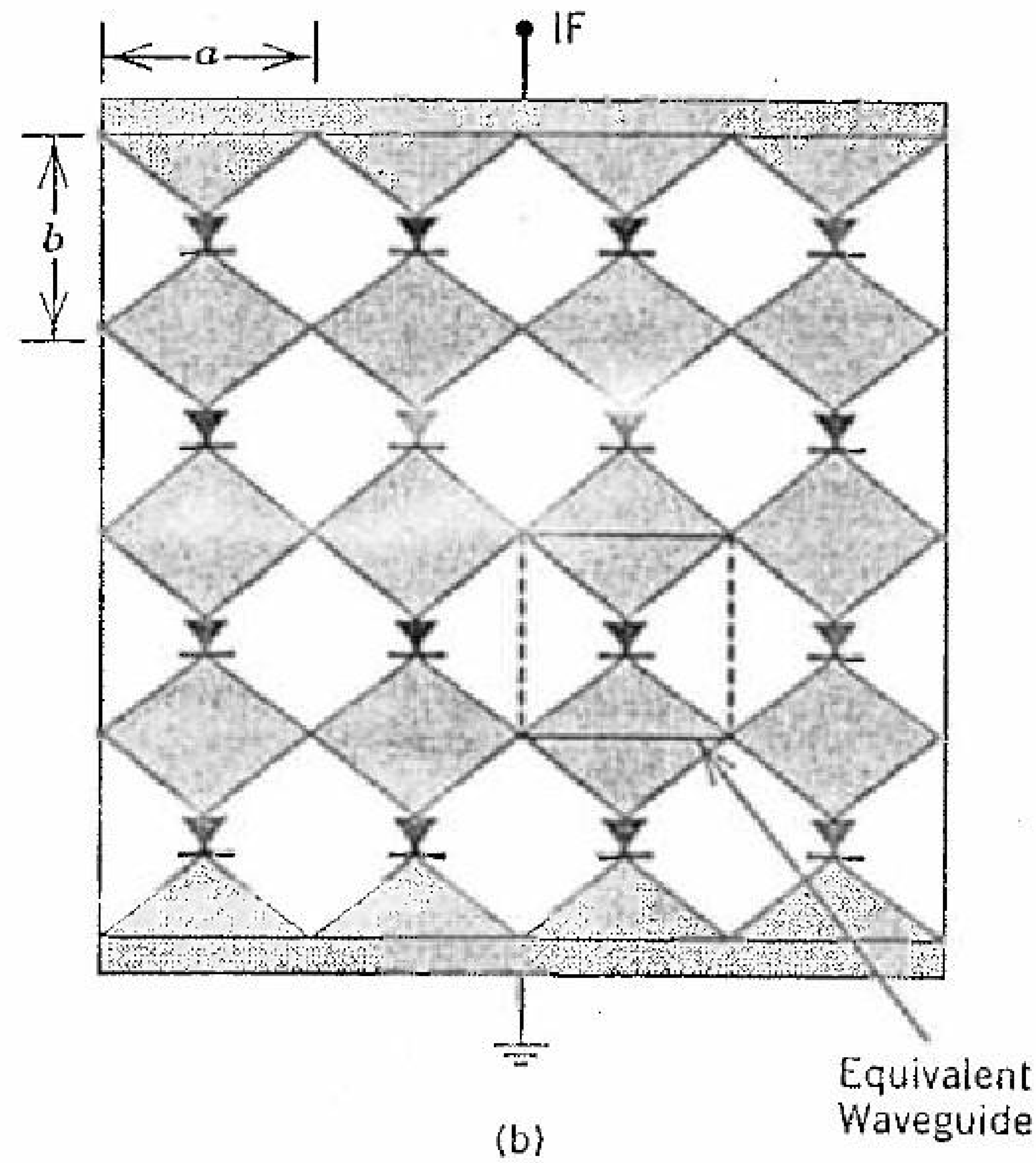


FIGURE 8.19 (a) Grid mixer with dipole-shaped metallization. The embedding impedance for this grid is primarily inductive. (b) Grid mixer with bow-tie-shaped metallization. The grid embedding impedance for the bow tie behaves like a short piece of transmission line.

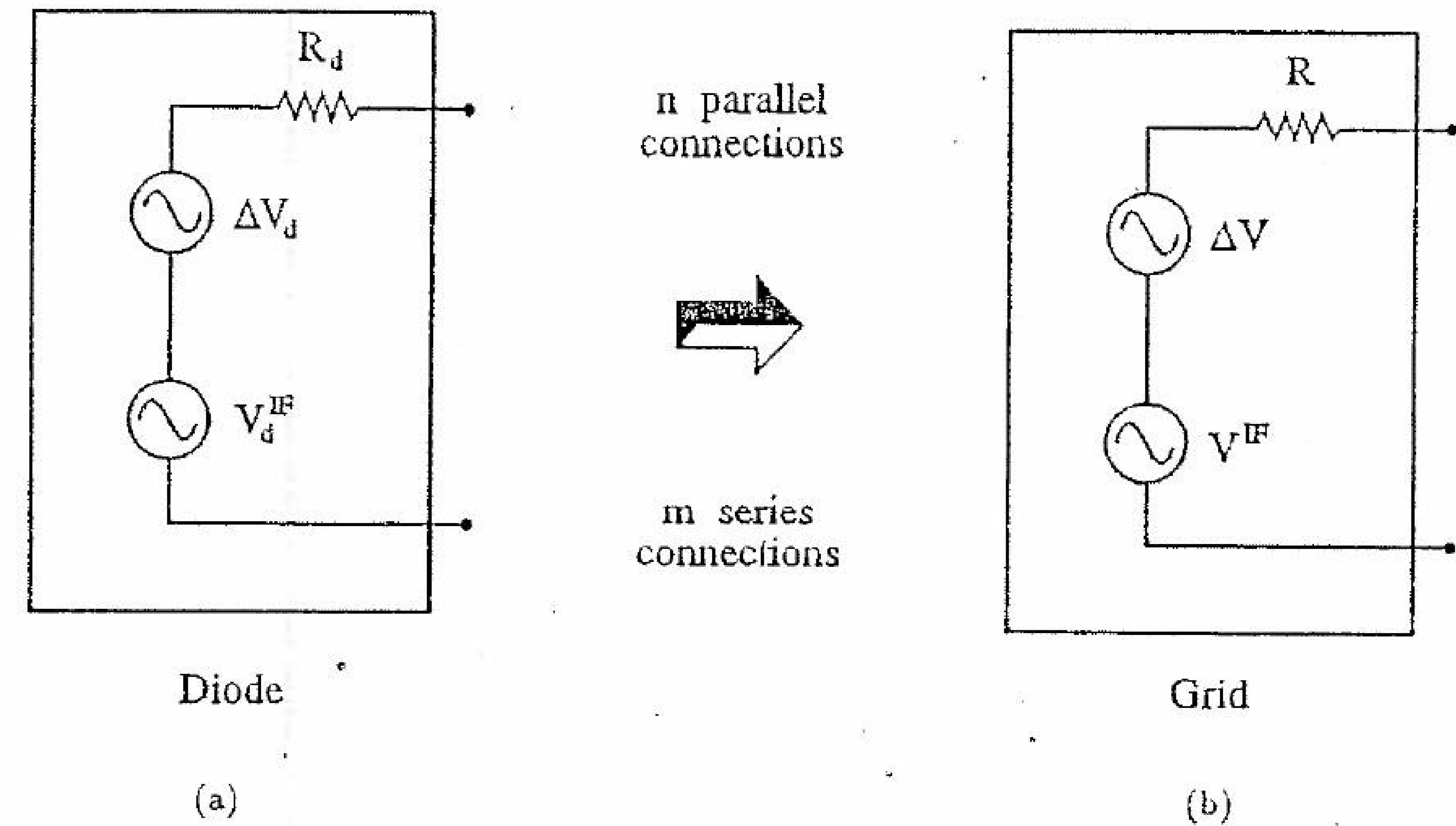


FIGURE 8.20 (a) Thevenin equivalent circuit for a single diode. (b) Thevenin equivalent circuit for the entire grid.

equivalent circuit for the grid, as shown in Figure 8.20(b), where the total resistance of the grid, R, is

$$R = R_d(m/n). \tag{8.21}$$

Assuming that the noise voltage of each diode is independent, the total noise voltage across a series connection of m diodes is

$$\sum^{m} \Delta V_d = \sqrt{m}\, \Delta V_d, \tag{8.22}$$

and consequently the noise voltage of the grid, ΔV, is

$$\Delta V = \Delta V_d \sqrt{m/n}\,, \tag{8.23}$$

from which it follows that the noise power of the grid, ΔP, is

$$\Delta P = \frac{\left(\Delta V_d \sqrt{m/n}\right)^2}{R_d(m/n)} = \Delta P_d. \tag{8.24}$$

From this we can conclude that the noise power of the grid is the same as that of an equivalent single diode. That is, the noise figure of the grid mixer is equal to the noise figure of a single-diode mixer placed in an equivalent embedding circuit.

A similar line of reasoning can be used to show that the conversion loss of the grid mixer is the same as that of an equivalent single diode. Namely, if P^{RF} is the available power of the incoming RF signal to be converted to the IF frequency, then for the single-diode case, using Eq. (8.19), we expect a converted IF power of

$$P_d^{IF} = \frac{P^{RF}}{L_C}. \tag{8.25}$$

The corresponding converted IF signal power for the $m \times n$ grid, P^{IF}, assuming the incoming RF power is distributed evenly among all the diodes in the grid, is

$$P^{IF} = \frac{(V^{IF})^2}{R} = \frac{(mV_d^{IF})^2}{R}$$
$$= \frac{m^2(R_d P^{RF}/L_C mn)}{R_d(m/n)} = \frac{P^{RF}}{L_C}. \tag{8.26}$$

Comparing Eqs. (8.25) and (8.26) shows that the converted IF power is the same for the single diode and the grid for a given RF signal power. In other words, the conversion loss of the grid mixer is the same as for a single diode with the same embedding impedance. We have done this analysis for the conversion loss for the IF, but the same reasoning holds for any mixing product. In particular, the ratio of the third-order intermodulation products to the IF power is, for the grid, the same as that for a single diode. However, the total power for the grid scales with the number of diodes. This means that the third-order intercept scales as the number of diodes in the grid.

Finally, it is worthwhile to compare the power handling of the grid mixer to an equivalent single-diode mixer. If we assume that the maximum RF input power that a single diode can safely handle is $\tilde{P}_d^{RF}$, and we assume uniform illumination of the grid mixer so that the incoming RF signal power is distributed evenly among all diodes in the grid, then for our $m \times n$ grid the maximum power handling of the grid mixer, $\tilde{P}^{RF}$, is simply

$$\tilde{P}^{RF} = mn\tilde{P}_d^{RF}. \tag{8.27}$$

In other words, the power-handling scales with the number of devices in the grid.

This reveals an important property of the grid mixer—its ability to increase dynamic range without compromising sensitivity. We have shown that since the RF power is spread among all the devices, the saturation power of the grid is increased by a factor of the number of devices. However, the noise figure of the grid remains equal to that of a single-diode mixer.

Consequently, the dynamic range is increased by a factor of the number of devices in the grid as well. Of course, the trade-off is that the required LO power is also raised by the same amount. This trade-off between dynamic range and LO power is one that occurs in virtually all mixers. The advantage of the grid is that we can increase the LO power, and hence dynamic range, virtually without limit by increasing the number of diodes in the grid. At the same time the conversion loss and noise figure of the grid can be independently optimized by adjusting the LO power per diode. This decoupling of sensitivity and power handling makes the grid mixer particularly attractive for mixers where power handling of the nonlinear element is fundamentally limited, such as the superconducting tunnel junction (SIS) mixer.

The primary disadvantage of the grid mixer is that in order to maintain the same LO power per diode, the total incident LO power on the grid must also be scaled with the number of diodes in the grid. Consequently, for large-grid mixers, a suitable high-power LO source must be available to get the best performance possible from the mixer diodes. One possible source suitable for the grid mixer LO is the power-grid oscillator discussed earlier. The grid oscillator output power also scales with the number of devices in the grid, so it is a natural counterpart to the grid mixer. It is also reasonable to think of using a chain of quasi-optical grid amplifiers as a high-power LO source (grid amplifiers are discussed in Section 8.5). With grid amplifiers, the signal source could even be a conventional low-power oscillator feeding a horn antenna, which would allow integration of an existing conventional LO into a quasi-optical receiver.

Two basic configurations can be used when designing a grid mixer. Depending on the application, the LO and RF signals may be combined quasi-optically before being directed onto the grid mixer surface, as shown in Figure 8.21. This has the advantage that if the grid is oriented so that the diode side faces the mirror, the substrate can then be used as an impedance transformer to improve the match between the diodes and free space. Alternatively, the LO and RF signals can be kept isolated from each other. For example, the RF might be incident from the back surface of the grid, and the LO signal incident from the front. Bandpass or notch-filter grids on either side of the grid mixer could then be used to isolate the LO from the RF, as shown in Figure 8.22. This design has the advantage that the grid mixer can be tuned to optimize the reflection coefficient at both the LO and RF frequencies independently by adjusting the properties and position of the bandpass filter grids. This design is also potentially more convenient for use in a quasi-optical receiver where the RF signal would first pass through a grid amplifier in front of the grid mixer, and the LO would be generated by an LO source and a chain of grid amplifiers or a grid oscillator behind the grid mixer.

Once the basic grid mixer configuration is established, the design of the unit-cell metal pattern must be considered. The choice of the unit-cell metal pattern affects the embedding impedance presented to the diode in the grid.

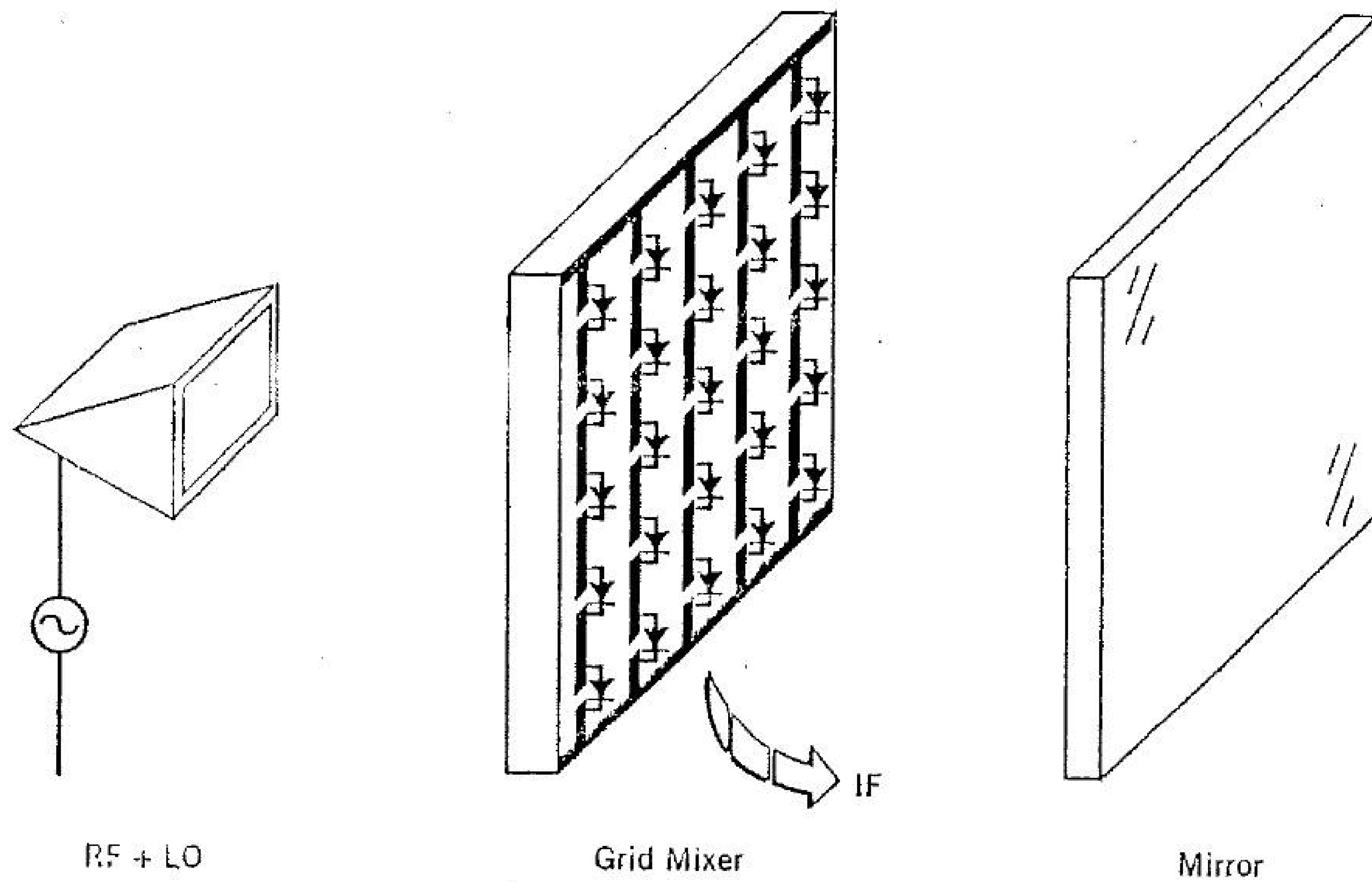


FIGURE 8.21 One-sided grid mixer configuration where the LO and RF signal beams are combined before being directed onto the grid mixer surface. In this case, LO and RF isolation is the responsibility of the external beam combiner.

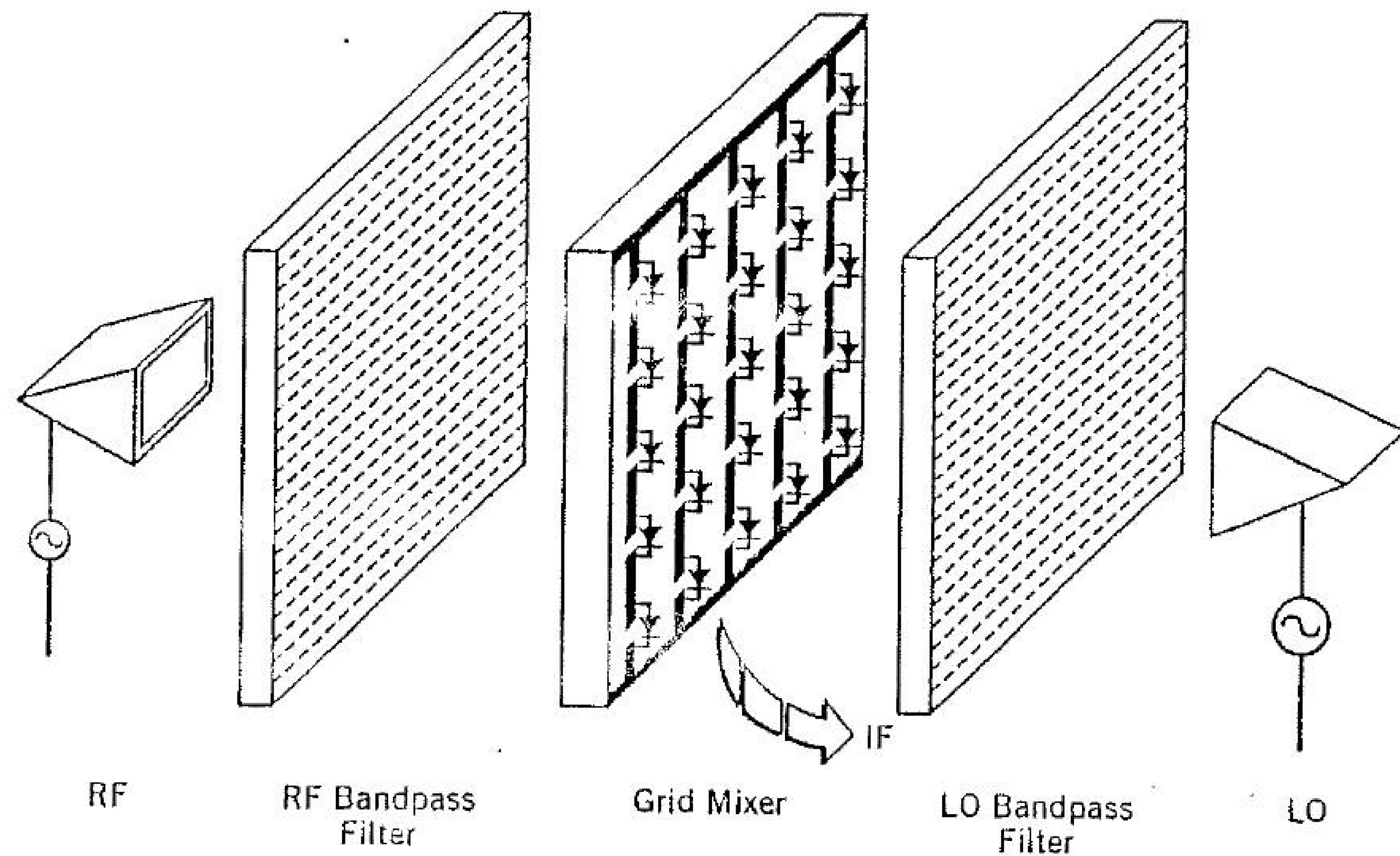


FIGURE 8.22 Two-sided grid mixer configuration where the LO and RF are kept separate and are incident on the front and back surfaces of the grid mixer respectively. Bandpass filter grids are used to isolate the LO and RF signal beams.

The use of narrow strips results in a predominantly inductive embedding impedance, which can be useful for resonating out the junction capacitance of the diode to obtain a better impedance match with free space. This results in a narrowband design that will typically have bandwidths on the order of a few percent of the fundamental frequency. Fortunately, at millimeter-wave frequencies this can still be several gigahertz.

If a bow-tie pattern is chosen, the grid embedding impedance resembles a shunt section of low-impedance transmission. The electrical length of the transmission line is only a fraction of a wavelength, making the bow tie suitable for broadband circuits if the diode has a small junction capacitance. In cases where bandwidth and impedance match are both critical, a combination of a bow tie and a strip can be used to help tune out diode capacitance without sacrificing too much bandwidth or excessively degrading grid return loss.

At the RF and LO frequencies the quasi-optical grid mixer can be modeled as a three-port network. Ports 1 and 2 are, respectively, the front and back of the grid itself, and the third port is the location in the grid unit cell where the diode is mounted. Obtaining the three-port scattering parameters of an arbitrary quasi-optical grid mixer is a challenging problem. To date, solutions for arbitrarily shaped unit-cell metal patterns are not available. However, significant progress has been made for specific metal patterns, such as bow ties and strips for grids assumed to be infinite in extent, by EMF analysis [12]. Solutions of this type, because they assume grids of infinite extent, completely ignore grid edge effects. Nevertheless, models based on such assumptions have been experimentally shown to provide good accuracy.

For a unit cell with a vertical strip of width w (Figure 8.23(a)), the equivalent circuit is a simple shunt inductor, L (Figure 8.23(b)), whose reactance can be computed as follows:

$$Z_L = \frac{2b}{a} \sum_{m=1}^{\infty} \cos^2\left(\frac{m\pi}{2}\right) \mathrm{sinc}^2\left(\frac{m\pi w}{2a}\right) \left(Z_{m0}^{TE+} \| Z_{m0}^{TE-}\right), \tag{8.28}$$

where $Z_0^{TEM} = \sqrt{\mu/\epsilon}$, $Z_{mn}^{TE} = \omega\mu/k_z$, and k_z, the propagation constant, is

$$k_z = \sqrt{\omega^2\mu\epsilon - \left(\frac{m\pi}{a}\right)^2 - \left(\frac{n\pi}{b}\right)^2}. \tag{8.29}$$

For a unit cell with a bow-tie metal pattern, shown in Figure 8.24(a), the equivalent circuit is a shunt transmission line of characteristic impedance Z_{BT} and electrical length θ_{BT}, as shown in Figure 8.24(b). These values are

$$Z_{BT} = \sqrt{\frac{Z}{Y}}, \tag{8.30}$$

$$\theta_{BT} = \sqrt{ZY}, \tag{8.31}$$

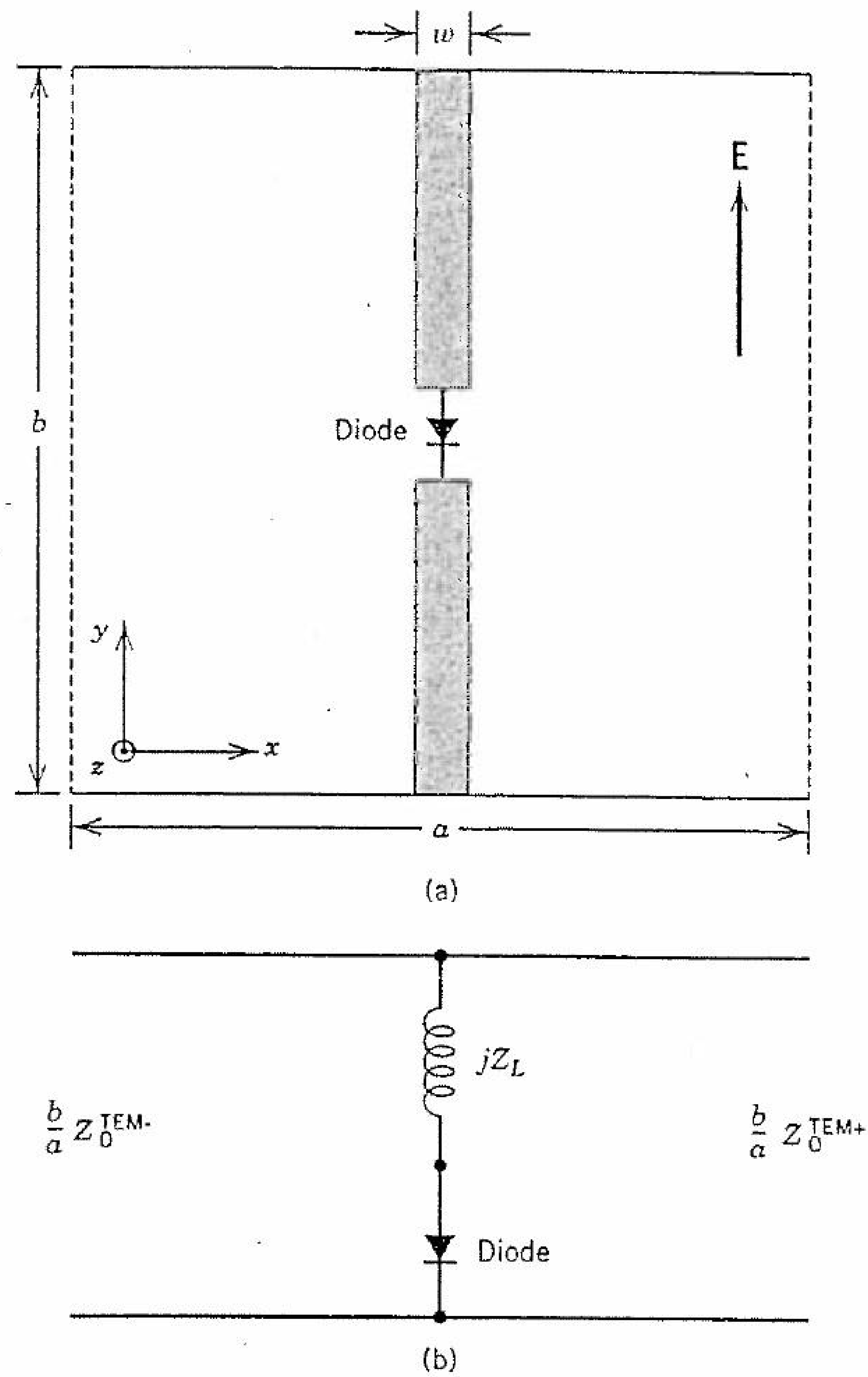


FIGURE 8.23 (a) Simple vertical-strip unit cell. Boundary conditions are imposed by the grid symmetry. The solid lines (—) are electric walls ($E_{tan} = 0$) and the dashed lines (---) are magnetic walls ($H_{tan} = 0$). (b) Simplified ECM for the vertical-strip grid mixer.

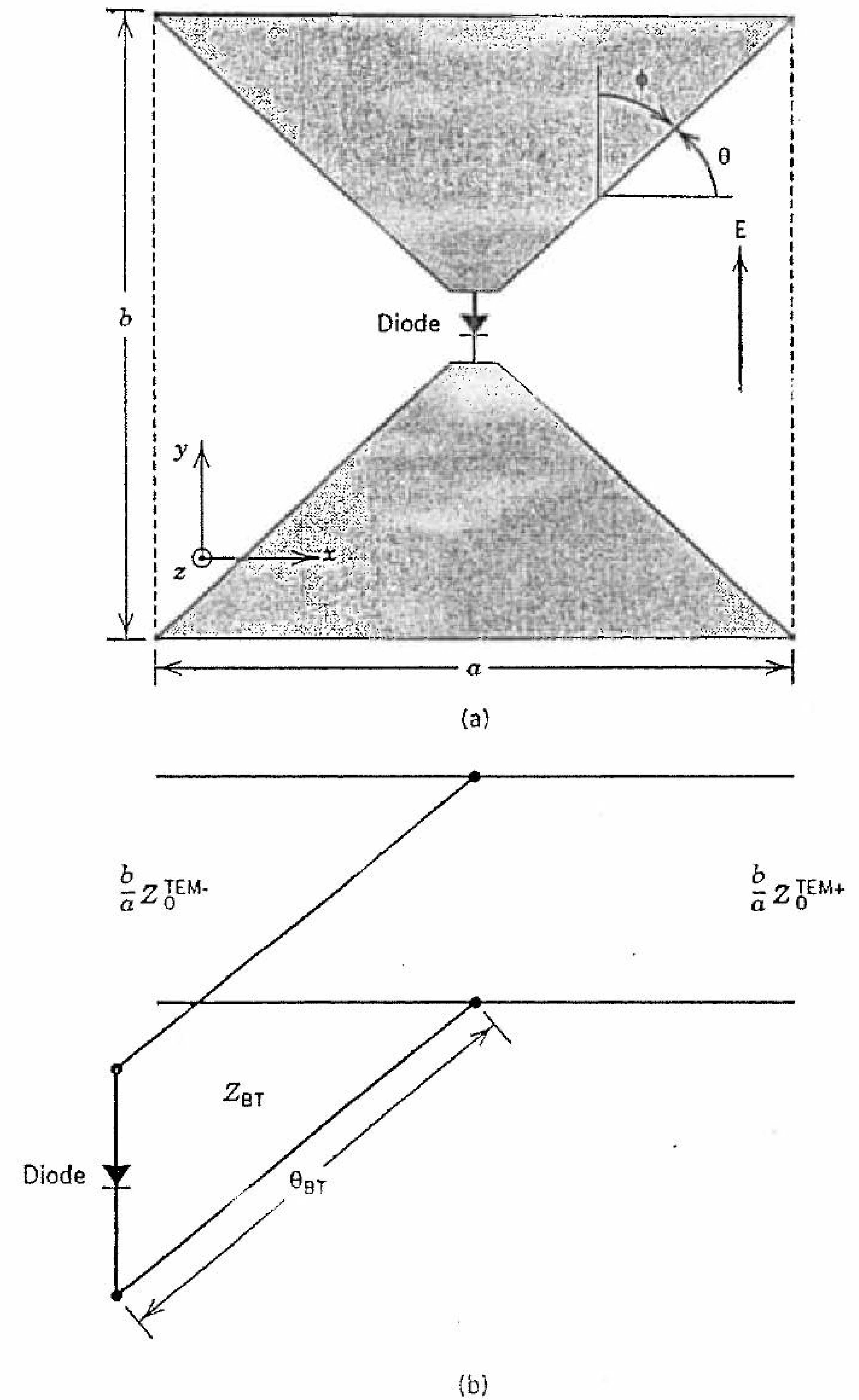


FIGURE 8.24 (a) Simple bow-tie unit cell. Boundary conditions are imposed by the grid symmetry. The solid lines (—) are electric walls ($E_{tan} = 0$) and the dashed lines (---) are magnetic walls ($H_{tan} = 0$). (b) Simplified ECM for the bow-tie grid mixer.

where

$$Z = \frac{1}{ab} \sum_{\substack{m=1 \\ n=0}}^{\infty} 2\epsilon_{0n} \frac{k_c^2}{k_x^2} A_{mn}^2 (Z_{mn}^{TE+} \| Z_{mn}^{TE-}), \tag{8.32}$$

$$A_{mn} = \frac{\displaystyle\int_0^b \int_0^\phi \frac{\cos(k_x y \tan\psi)}{\sqrt{\sin^2\phi - \sin^2\psi}} \cos k_y y \, d\psi \, dy}{\displaystyle\int_0^\phi \frac{d\psi}{\sqrt{\sin^2\phi - \sin^2\psi}}}, \tag{8.33}$$

$$Y = \frac{1}{ab} \sum_{\substack{m=0 \\ n=1}}^{\infty} 2\epsilon_{m0} \frac{k_c^2}{k_y^2} B_{mn}^2 (Y_{mn}^{TM+} + Y_{mn}^{TM-}), \tag{8.34}$$

$$B_{mn} = \frac{\displaystyle\int_0^a \int_0^\theta \frac{\cos(k_y x \tan\xi)}{\sqrt{\sin^2\theta - \sin^2\xi}} \cos k_x x \, d\xi \, dx}{\displaystyle\int_0^\theta \frac{d\xi}{\sqrt{\sin^2\theta - \sin^2\xi}}}, \tag{8.35}$$

and $Y_{mn}^{TM} = \omega\epsilon/k_z$, $k_x = m\pi/a$, $k_y = n\pi/b$, $k_c^2 = k_x^2 + k_y^2$, and

$$\epsilon_{mn} = \begin{cases} 1, & \text{if } m = n, \\ 2, & \text{otherwise.} \end{cases} \tag{8.36}$$

For design purposes, we generally want to find the reflection coefficient of an infinite grid for a plane wave at normal incidence on the front surface of the grid. For this discussion, it is reasonable to assume that we have the configuration shown in Figure 8.21—that is, a mirror behind the grid with the diodes facing the mirror. The two-sided grid mixer in Figure 8.22 can be handled similarly; one need only add the two-port S-parameters of the bandpass filter grids to complete the model.

The equivalent circuit for the grid mixer with a mirror a distance d behind the grid is shown in Figure 8.25, where the circuit in part (a) is for a vertical-strip unit cell and the circuit in part (b) is for a bow-tie-shaped unit cell. As described earlier, the grid is modeled as a three-port network. Ports 1 and 2 are respectively the front and back of the grid, and the third port is defined at the diode terminals, where the diode is mounted to the grid. The incident LO + RF TEM mode signal is modeled as a 377-Ω source connected to port 1. The mirror placed behind the grid terminates port 2 in a short-circuited stub, and port 3 is terminated by the mixer diode. The entire grid is in this way reduced to a one-port equivalent circuit. A transmission line represents the propagating TEM mode as it passes through the substrate that supports the grid. As mentioned, the bow-tie grid is modeled as a short

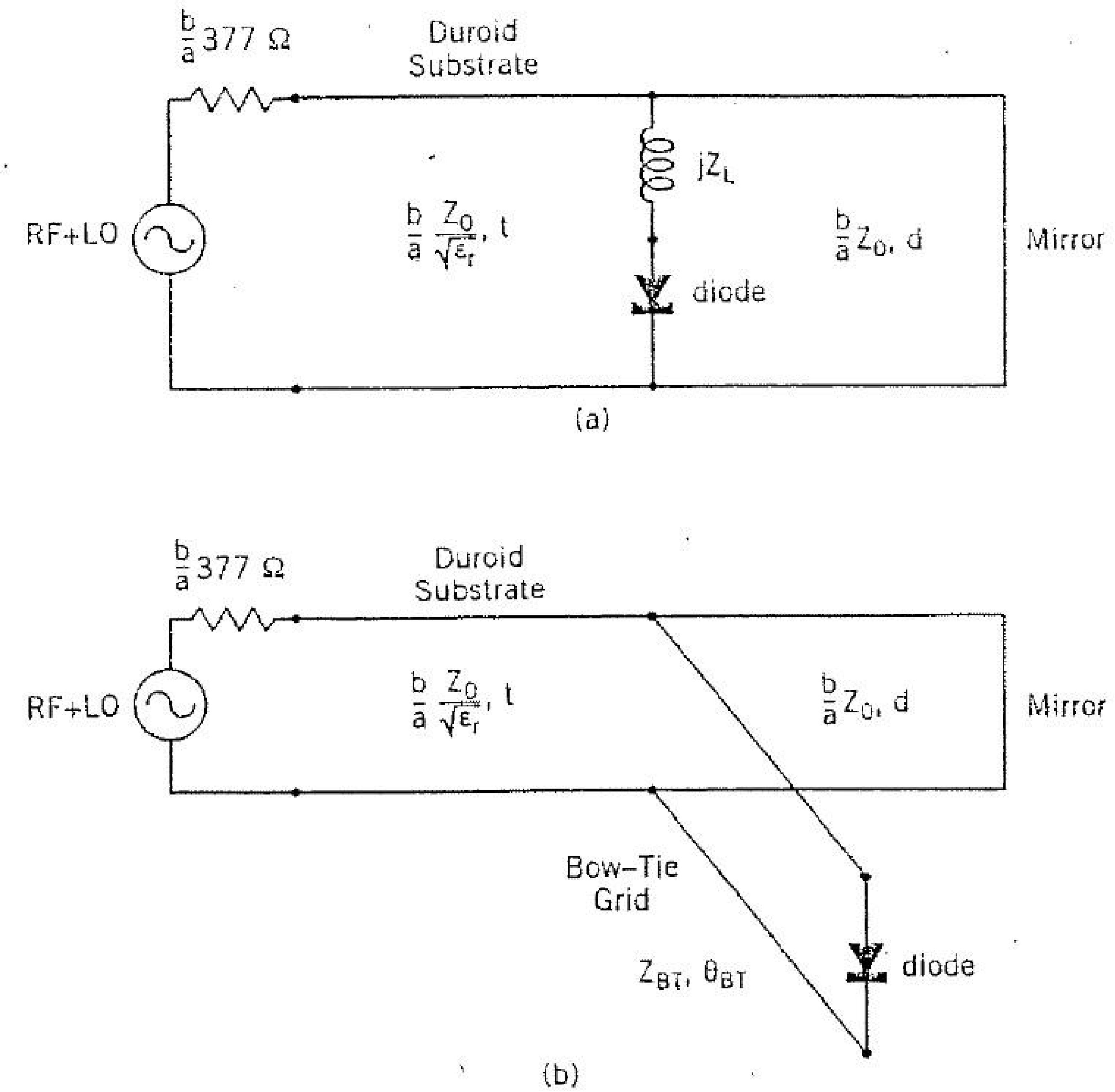


FIGURE 8.25 (a) Transmission line model for the grid configuration of Figure 8.21 with (a) vertical-strip unit-cell metal pattern, (b) bow-tie unit-cell metal pattern.

section of transmission line with characteristic impedance Z_{BT} and electrical length θ_{BT}. Values for Z_{BT} and θ_{BT} are obtained from Eqs. (8.30) and (8.31), derived using EMF analysis. Similarly, the strip is modeled as a shunt inductor with reactance Z_L, given by Eq. (8.28).

The diode is added to the grid model by using the manufacturer's equivalent circuit. Modeling the nonlinear behavior of a mixer diode is a difficult problem, and most of the popular commercially available harmonic balance software is inadequate for accurately characterizing the behavior of mixers. To make matters worse, the models used by such software are almost always proprietary. Fortunately, most diode manufacturers provide a linear equivalent circuit for the RF and LO frequencies that can be used to design efficient matching networks to give good mixer performance. Such simple linear models cannot be used to predict conversion loss or intermodulation characteristics of the mixer, but they are useful when designing the RF, LO, and IF sections of the mixer embedding network.

Simulation of the grid is carried out by calculating the reflection coefficient the grid presents to the RF and LO source connected to port 1. The

design is optimized by matching the grid impedance to free space (377 Ω) at the design frequency of the mixer. In the bow-tie grid, the S-parameters of the short section of transmission line with characteristic impedance Z_{BT} and electrical length θ_{BT} used to model the bow tie can be computed from Eqs. (8.30) and (8.31), derived using EMF analysis. Appendix B lists a C++ program for computing the EMF-derived S-parameters of the bow-tie grid over the frequency range of interest. Although the algorithm is computationally more intensive than for the crossed-dipole case described earlier for the grid oscillator, results can still be obtained within minutes running on nothing more than a 386 class personal computer. Similarly, the strip can be modeled as a shunt inductor with reactance Z_L, given by Eq. (8.28). The C++ program listing in Appendix A for the crossed-dipole unit cell includes the computation of the S-parameters of the strip as a necessary part of the computation of the more complex crossed-dipole pattern, and is thus suitable for modeling the simpler vertical strip for inclusion in the grid mixer model.

To complete the simulation, we insert the S-parameters into the ECM and compute the grid port 1 reflection coefficient, using traditional linear circuit analysis. If the analysis shows the grid impedance is not matched to free space (377 Ω) at the design frequency for any reasonable mirror position, then the grid unit-cell size, lead dimensions, and substrate thickness can be adjusted in an iterative fashion until the grid is matched at the desired frequency. Typically, a commercial linear microwave design package would be used for the simulations. The fast computation of the grid element S-parameters using the EMF solution allows many iterations of the design cycle to be performed in a very short time.

Because a design based on the EMF method alone is likely to contain uncertainties of up to 10% of the simulated results, it may be desirable to simulate the grid unit cell, designed using the EMF method, with a potentially more accurate technique, such as a commercial finite-element electromagnetic solver, or a MOM analysis to further fine-tune the design before fabrication. This is particularly important if the grid metallization pattern differs significantly from the simple bow-tie or strip solutions presented here.

An experimental X-band grid mixer built to test the theoretical performance improvements of the quasi-optical grid mixer concept is shown in Figure 8.26. This grid consists of 100 low-barrier Schottky beam-lead diodes epoxied to a Duroid microwave substrate with a bow-tie-shaped cell metal pattern [26].

Figure 8.27 shows the measured conversion loss of the grid mixer as a function of LO power per diode for combined LO and RF signals normally incident on the grid. Figure 8.27 also shows the measured conversion loss of an equivalent single-diode microstrip mixer. The results verify that the grid mixer conversion loss is nearly equal to the single-diode mixer. The difference can be attributed to the slightly unequal impedances presented to the diodes for the two mixer designs.

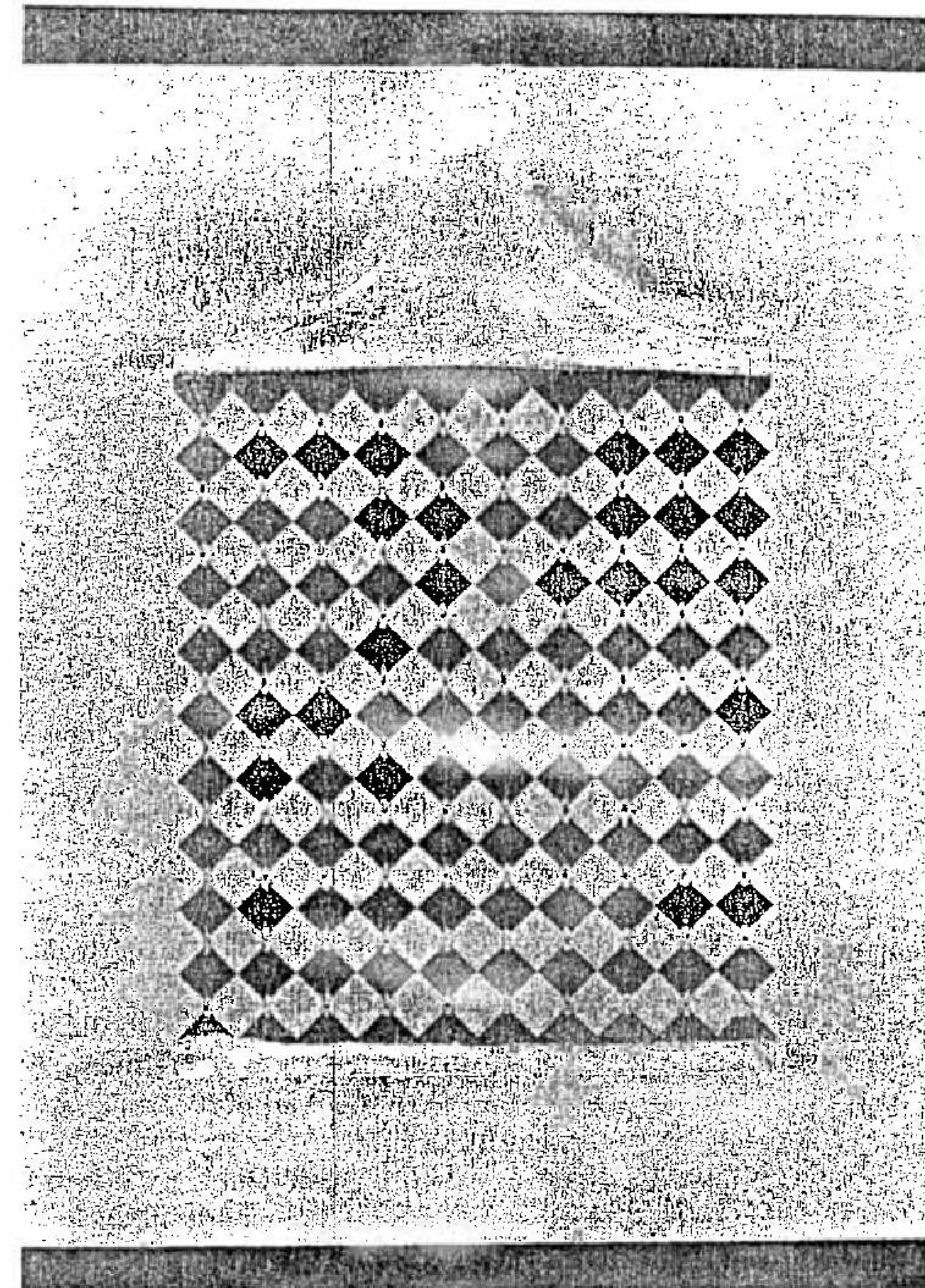


FIGURE 8.26 A 100-element X-band grid mixer. The unit cell width is 3 mm. The incident RF and LO electric fields are polarized vertically. The IF signal is taken off the top and bottom edges of the grid. The diodes are bonded to the grid with silver epoxy.

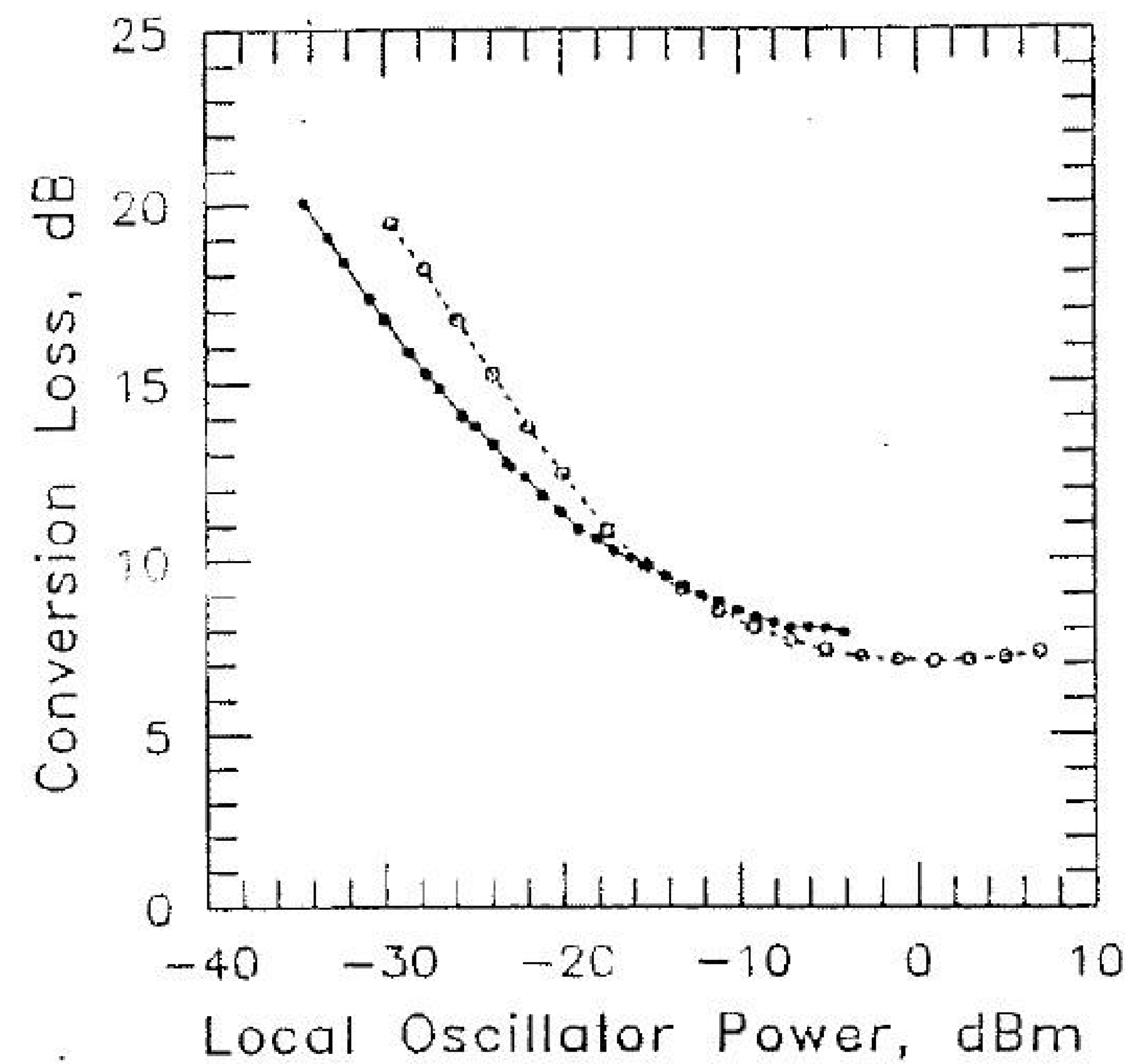


FIGURE 8.27 Measured grid mixer conversion loss (—) and equivalent single-diode mixer conversion loss (---) as a function of LO power per diode. The conversion loss of the grid mixer is comparable to an equivalent single-diode mixer.

The third-order intercept point is the power at which the undesired third-order intermodulation products are equal to the power of the desired signal. For a mixer, power is typically defined to be the input RF power of one of the desired signals, denoted P_{REF}. The third-order intermodulation distortion products are typically measured relative to the desired IF signal, denoted IMD_3. Since the power of the third-order intermodulation distortion products increases three times faster than the desired signals, from these two measurements the extrapolated power at which the desired and undesired signals will have the same power, the third-order intercept point, can be computed from the equation

$$IP_3 = P_{REF} + \frac{IMD_3}{2}. \tag{8.37}$$

The linearity of a diode is a function of LO power, P_{LO}. For this reason, it is essential that we compare the single-diode mixer linearity with the grid mixer, using the same LO power per diode. Figure 8.28(a) shows the measured third-order intercept point for the grid and single-diode mixers. Figure 8.28(b) shows the difference in third-order intercept point for the two mixers. Improvements of 16.3 to 19.8 dB were measured over a 30-dB range of LO powers. This compares favorably with the expected improvement of 20 dB predicted from theory for a 100-element grid.

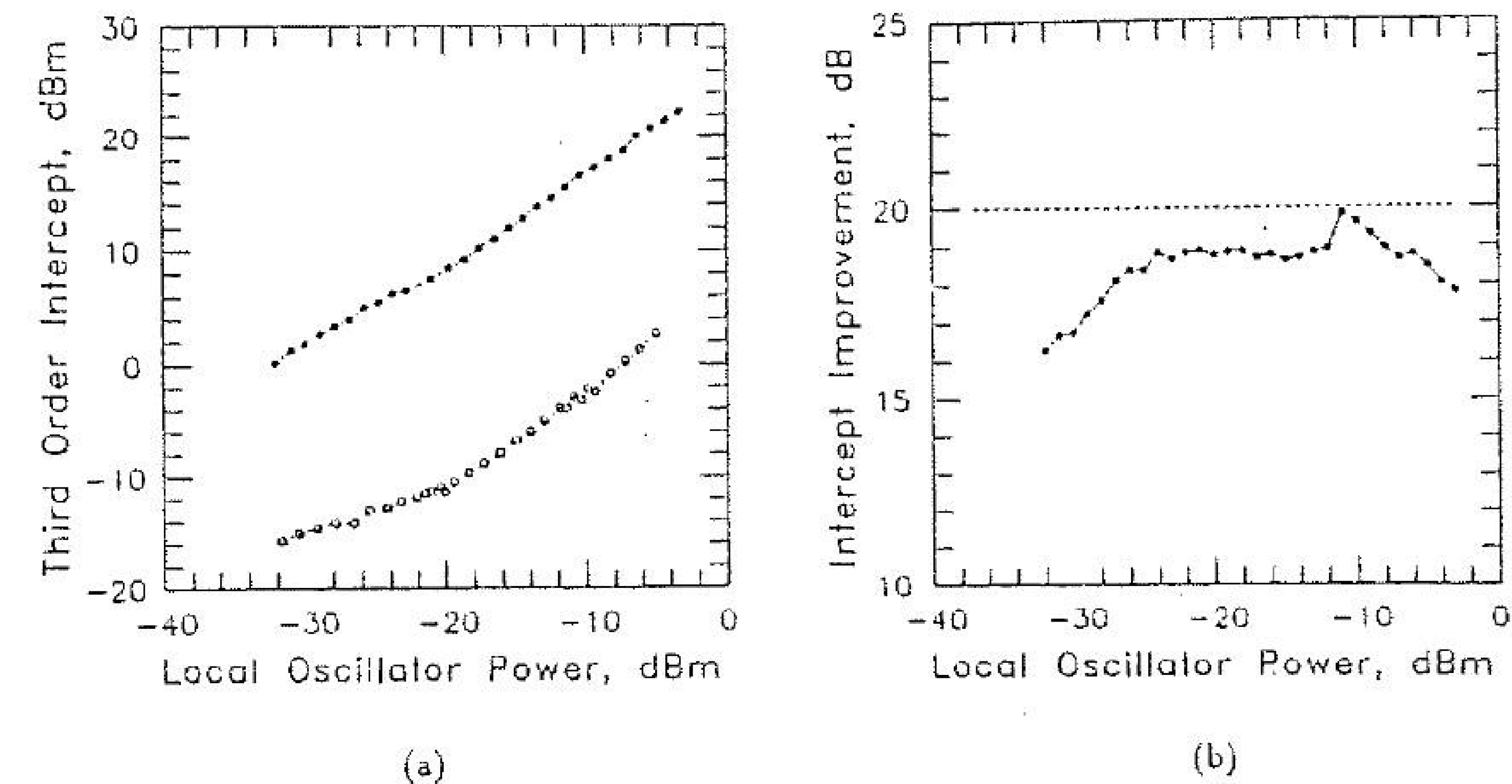


FIGURE 8.28 (a) Measured grid mixer third-order intercept point (—) and equivalent single-diode mixer third-order intercept point (---) as a function of local oscillator power per diode. (b) Measured improvement in third-order intercept point for the grid mixer over the single-diode mixer (—) as a function of local oscillator power per diode. Theory (---) predicts a 20-dB improvement for a 100-element grid.

8.5 GRID AMPLIFIERS

Although they are important for many millimeter- and submillimeter-wave systems, oscillators are only one possible use for transistor grids. Amplifiers —which are difficult to build at millimeter- and submillimeter-wave frequencies—are often necessary in many applications. Grid amplifiers offer the same advantages as grid oscillators: increased power-handling capability and elimination of the losses associated with waveguides and feed networks. In essence, a grid amplifier is a planar structure that radiates an amplified version of a wave incident on its surface. As a result, the grid design must accommodate an array of transistors and suppress potential spurious oscillations. In addition, there needs to be a means of isolating the output wave from the input wave.

Figure 8.29 illustrates the concept. The grid receives radiation polarized along the y direction and radiates a horizontally polarized wave. Polarizing plates are placed on either side of the grid to provide isolation between the amplifier input and output. The polarizers are thin circuit boards with conductive strips. This configuration helps to prevent the grid from oscillating and allows the polarizers to tune the input and output independently.

The unit cell of the grid contains a pair of transistors joined at the sources in the case of FETs, or emitters in the case of bipolar transistors, to form a differentially connected pair. Vertical metal leads are attached to the differ-

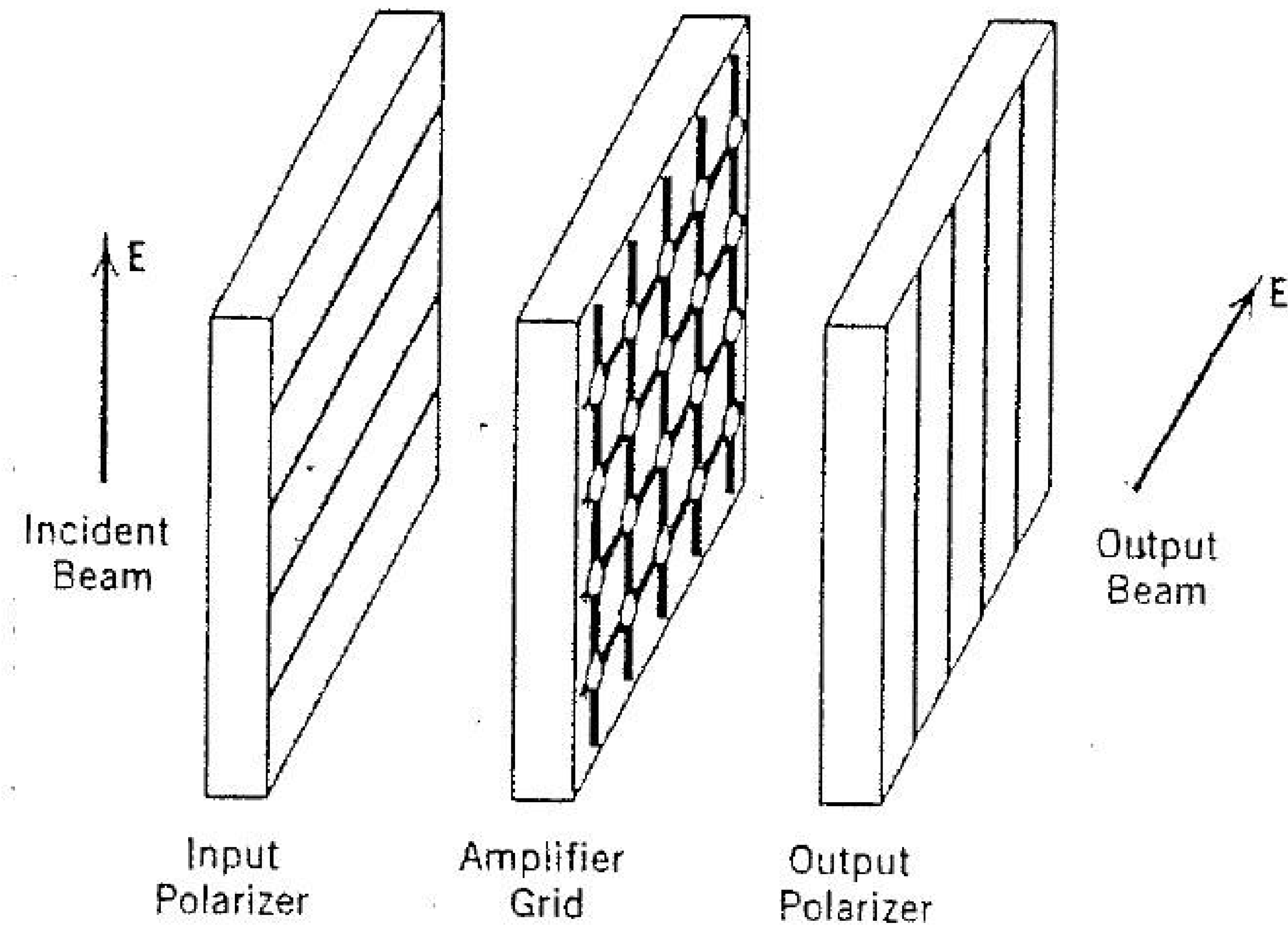


FIGURE 8.29 A grid amplifier. The input beam is vertically polarized and the output beam is horizontally polarized. The metal strips on the grid couple the beam to the active devices and radiate an amplified beam through the output polarizer.

ential-pair inputs, and horizontal leads connect to the outputs. The vertical leads pick up the incident radiation. The amplified signal radiates from the horizontal drain leads. A substrate supports the array while dc bias is applied to lines running horizontally across the substrate. To eliminate spurious common-mode oscillations, we place resistors between the transistor source or emitter leads and dc ground.

Amplifier gain is measured by illuminating the grid with vertically polarized radiation and measuring the power radiated in the orthogonal polarization. An expression for the amplifier gain is

$$G = \frac{P_r}{P_c}\left(\frac{\lambda r}{2A}\right)^2, \tag{8.38}$$

where P_r is the received power with the amplifier grid in place, P_c is the received power with the amplifier grid removed, A is the geometric area of the grid, and r is the distance between the grid and each horn. This simple formula allows the gain to be calculated from a relative power measurement and three well-known parameters.

The grid gain and the input and output return loss can also be measured with a quasi-optical network analyzer with focusing lenses. Typically, the measurement setup includes a microwave network analyzer, two feed horns, and two Teflon lenses. To measure the amplifier gain, one first calibrates the system for transmission loss by using an absorber screen with a square hole to

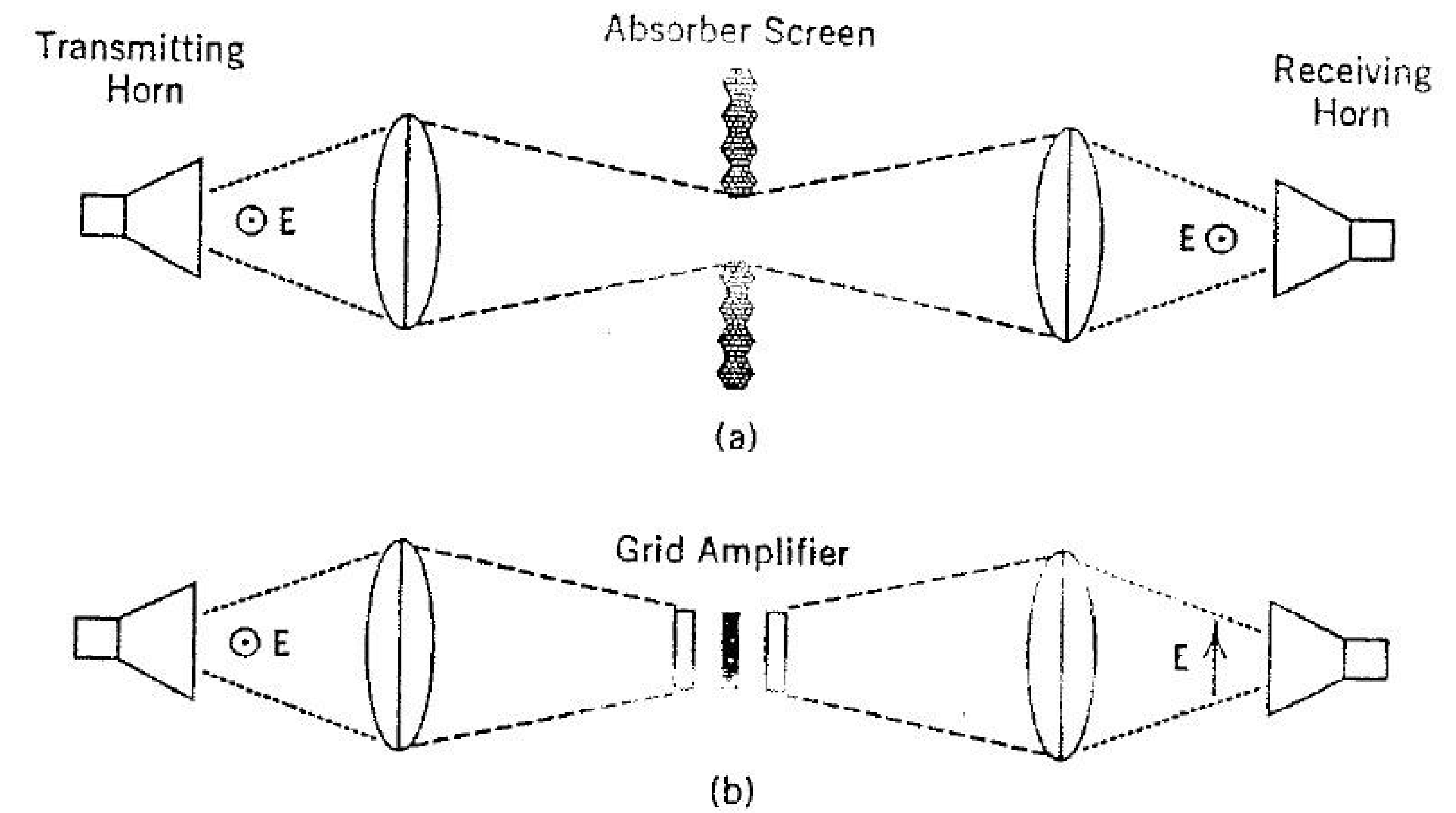


FIGURE 8.30 Quasi-optical gain measurements with focusing lenses: (a) transmission loss calibration; (b) amplifier gain measurement.

match the amplifier grid (Figure 8.30(a)). After calibration the amplifier grid is inserted, and the receiving horn is rotated 90° to match the amplified beam polarization (Figure 8.30(b)). The absorber is not required around the amplifier grid because the transmitting horn and the receiving horn are cross-polarized.

The first demonstrated grid amplifier was a device with 25 pairs of packaged MESFETs [27]. The transistors were wired as differential pairs with the two sources tied together. The two gates were the inputs, and the two drains were the outputs. It had metal strips on the back for biasing, and resistors and pins to connect to packaged transistors on the front. The strips were necessary for bias, but they also caused the grid to have a 3-dB bandwidth of only 3%. This configuration was also not a good candidate for future monolithic integration. Furthermore, because the transistors were packaged devices, the unit cell was forced to be large, restricting operation to a relatively low frequency.

Figure 8.31 shows the measured gain of the 25-element MESFET amplifier grid. A maximum gain of 11 dB occurs at 3.3 GHz. The input and output polarizers, which are likely responsible for the narrow (90 MHz) bandwidth, are important; gain is not observed without them. For comparison, the grid response when dc bias is removed is also shown in Figure 8.31.

Planar amplifier grids with up to 100 differential-pair elements have also been demonstrated with custom heterojunction bipolar transistor (HBT) chips [15]. The differential-pair HBT chip used in these amplifier grids is shown in Figure 8.32. The 1.7-kΩ resistors provide bias to the base, so there are only two external bias connections. They also provide negative feedback to help stabilize the grid. In addition, there are a pair of parallel 500-Ω

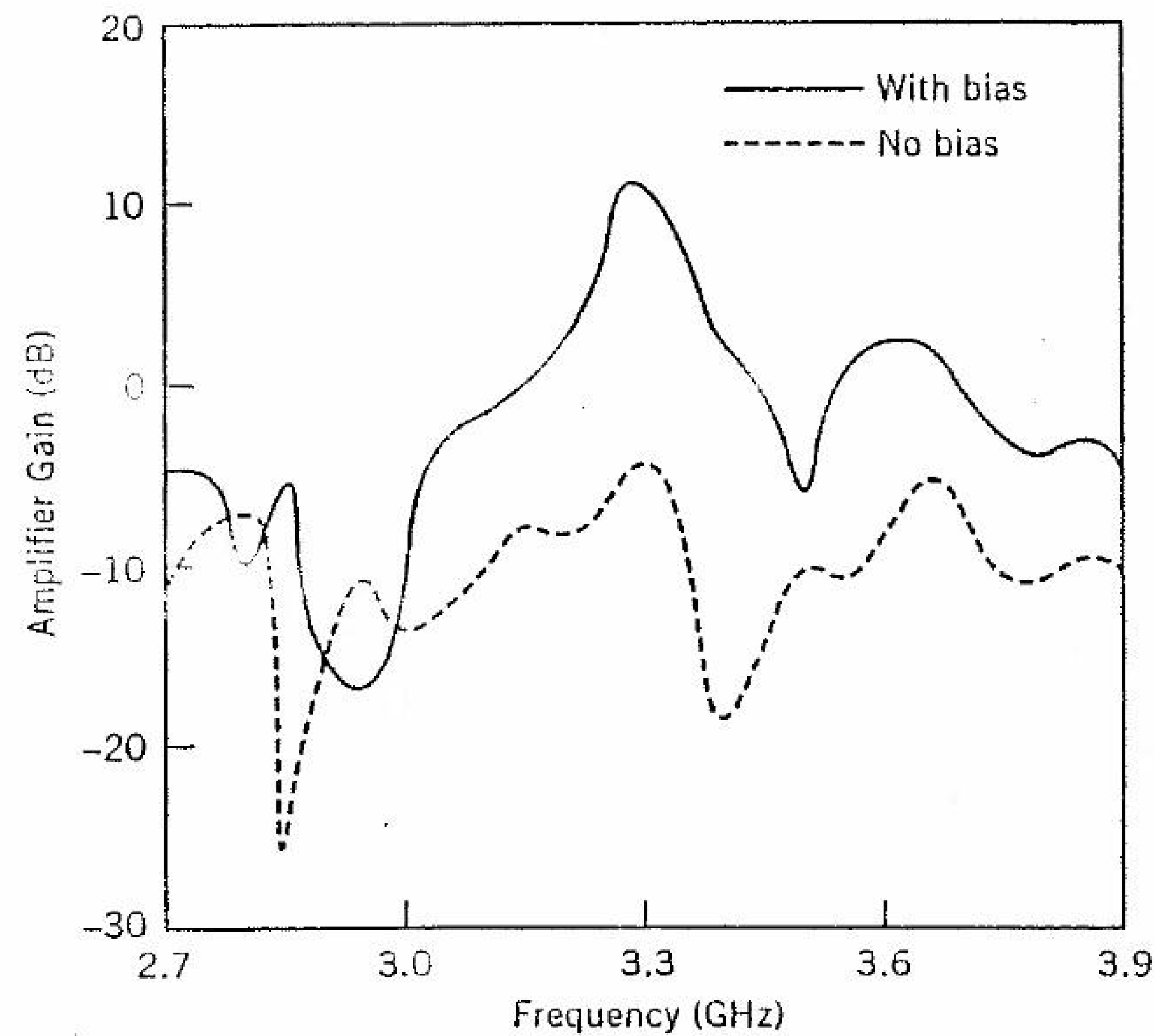


FIGURE 8.31 Measured grid amplifier gain with bias (solid line) and without (dashed line) for the 25-element MESFET grid. The total incident power was about 300 μW.

emitter resistors to reduce the common-mode gain to prevent the grid from oscillating.

Figure 8.33 shows the unit-cell pattern for a planar-grid amplifier. The metal structure in the grid has two parts: RF coupling for the input and output, and bias for the HBT chips. For input and output coupling, inductive strips are attractive because they are strongly polarized, providing good isolation between the input and the output to prevent unwanted oscillations. If large bandwidths are required, other metal patterns, such as the bow tie, could also be considered. Ideally, the bias lines should have a large reactance so as not to disturb the input and output beams. Consequently, narrow meander lines are used to provide bias. The meander lines were chosen because they have an inductive reactance approximately twice as large as a straight strip of the same length. A narrow capacitive gap is etched in the input strips to tune out inductance to get a better input impedance match.

The grid gain and the input and output return loss for a 100-element planar-grid amplifier are shown in Figures 8.34 and 8.35, respectively. The measurements were made with a quasi-optical network analyzer with focusing lenses. The results show that the peak gain was 10 dB at 10 GHz with a 3-dB bandwidth of 1 GHz. The peak could be shifted from 8 to 11 GHz by adjusting the polarizers. With no bias, the gain dropped below −8 dB everywhere. The standards used to calibrate the system for return loss were an absorber load, a metal short, and an offset short. The results in Figure

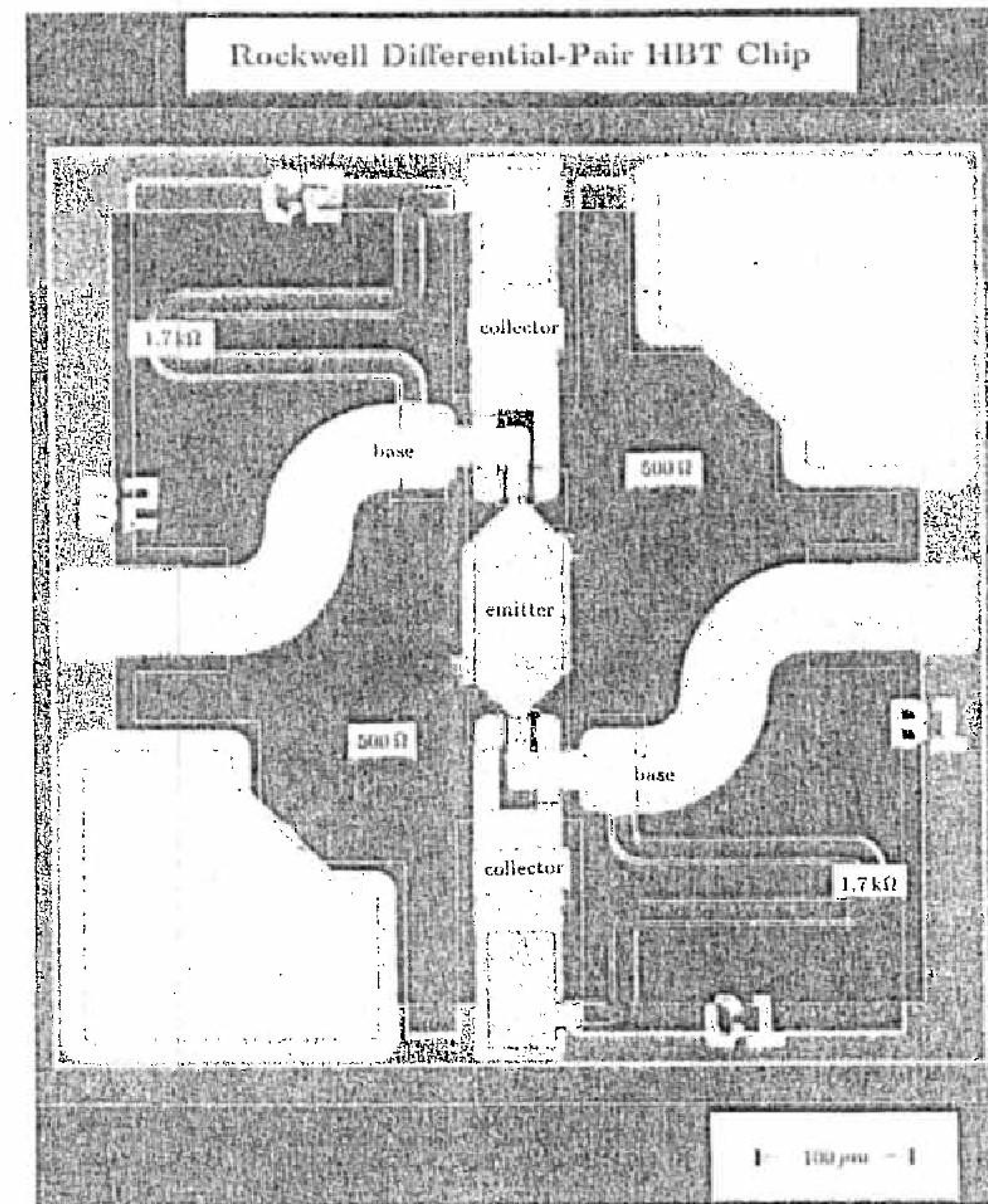


FIGURE 8.32 The differential-pair HBT chip layout.

9.35 indicate that the input and output return losses were better than 15 dB at 10 GHz.

A grid amplifier is a multimode device and can amplify beams at different angles. For example, it should be possible to place a grid amplifier after an electronic beam-steering array. The grid would amplify single and multiple transmitted beams while preserving propagation angles, side-lobe levels, and monopulse nulls. The amplifier could overcome losses in the beam steerer itself. A grid amplifier could also precede a receiving beam-steering array, allowing the noise performance to be determined by the grid rather than by losses in the beam steerer.

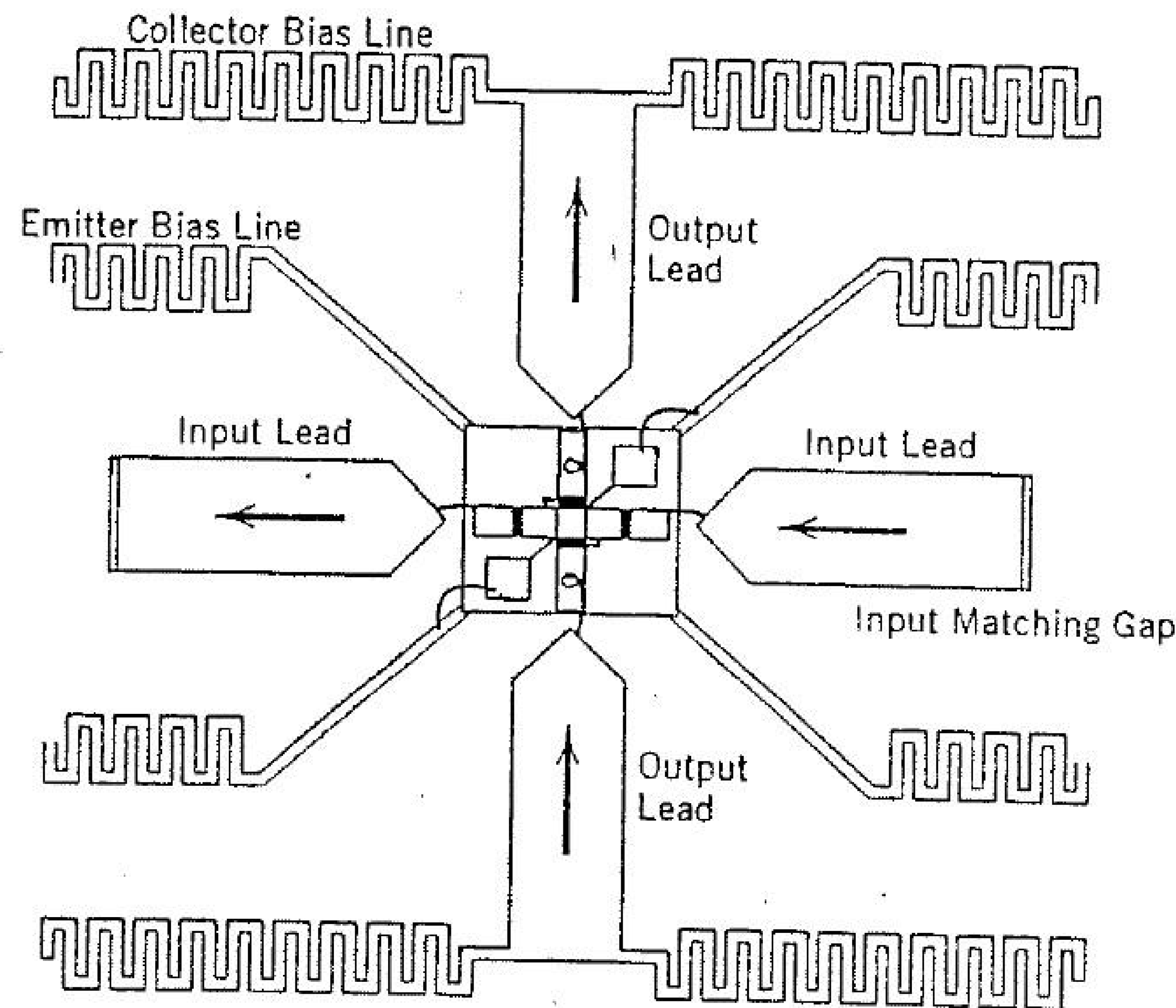


FIGURE 8.33 Grid amplifier unit-cell design. The arrows indicate the direction of current flow.

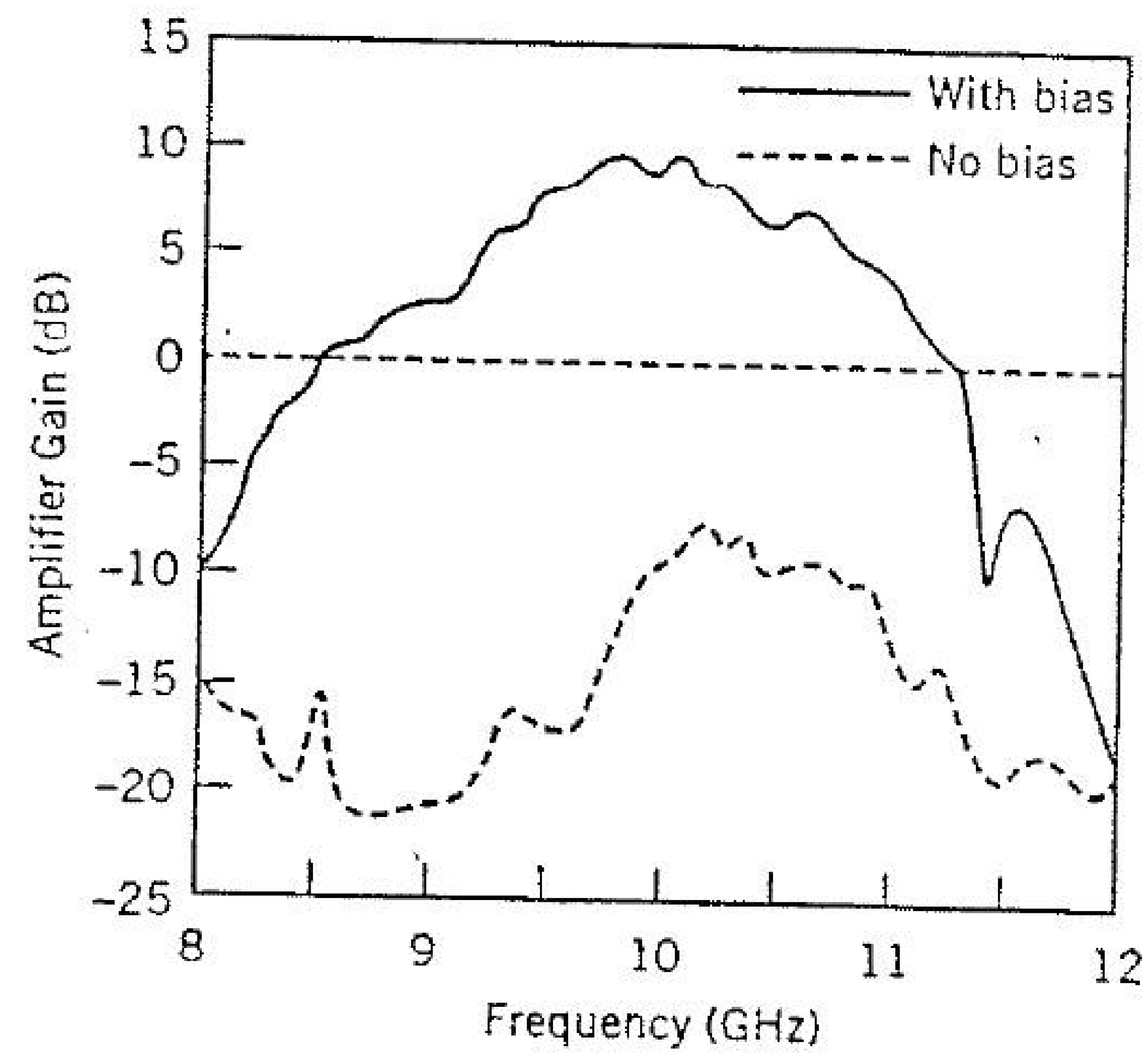


FIGURE 8.34 Planar-grid amplifier gain vs. frequency. The peak is 10 dB at 10 GHz. The 3-dB gain bandwidth is 1 GHz.

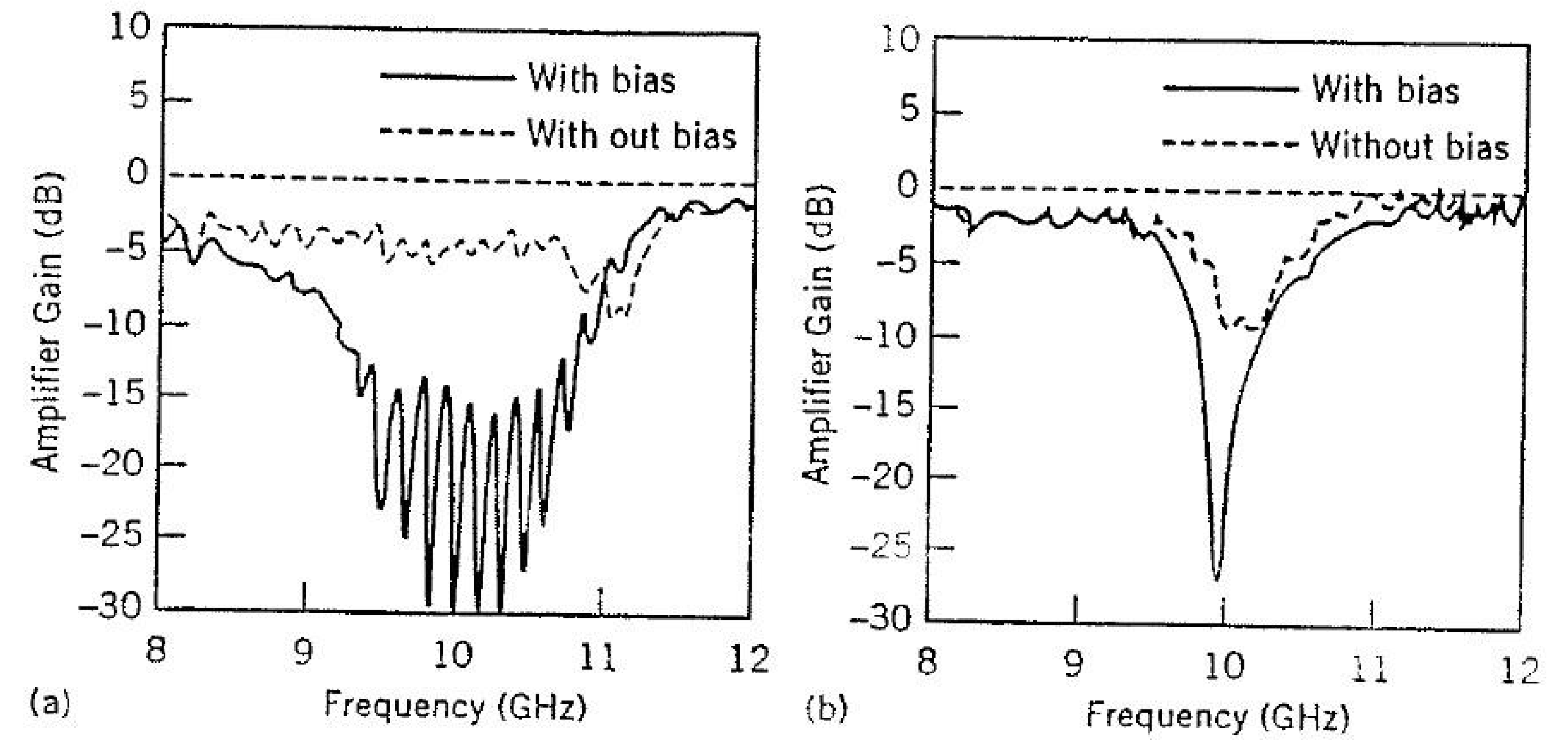


FIGURE 8.35 Planar-grid amplifier (a) input and (b) output return loss. The ripple in the input plot indicates that some reflected component was not accurately corrected for.

This multimode behavior is shown in the patterns of Figure 8.36(a) for a 100-element planar-grid amplifier with beams incident at 0°, +20°, and −20° angles. The peaks in the output beams are within 1° of the incident angles. The beams are all of similar width, and the side lobes are all at about the 13-dB level that we would expect for a uniformly illuminated aperture. Figure 8.36(b) shows the effect of rotating the grid with the input and output beams fixed. This measures the change in gain for different angles of incidence. The gain drops less than 3 dB for angles of incidence less than 30°. The primary cause of this drop in gain at extreme angles is changing beam

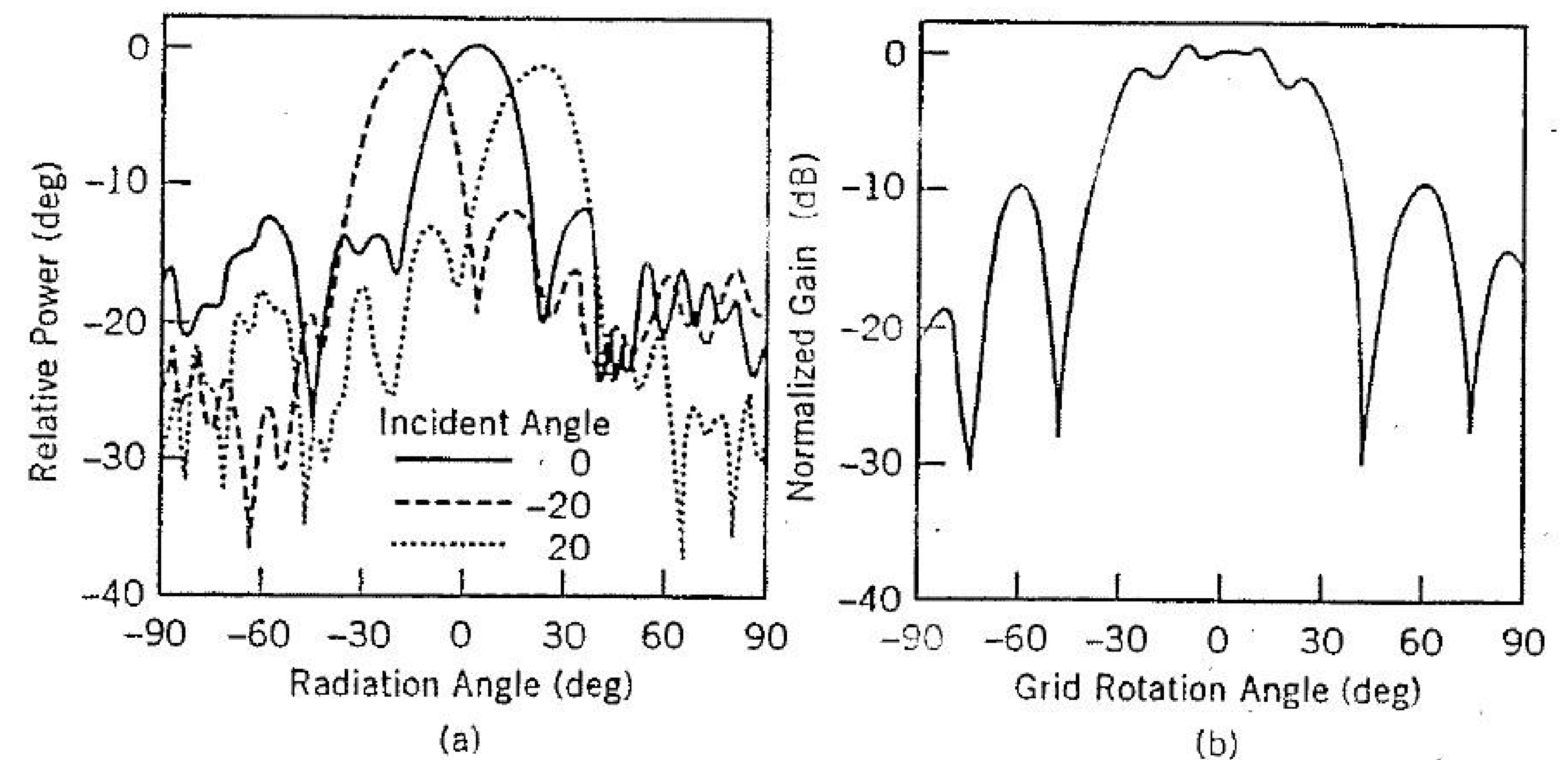


FIGURE 8.36 Amplifying beams at angles. (a) The grid amplifier radiation patterns for three incident beams. (b) Gain variation with incidence angle.

impedance. However, part of the loss is due to the fact that less power is being intercepted by the grid at oblique angles. This obliquity factor shows up in both transmitting and receiving space-loss factors, so we expect a $\cos^2 \theta$ loss (1.2 dB at 30°) in addition to the drop caused by changing impedances. Obliquity loss can be avoided in applications where the grid can be made larger than the beam.

A key issue in any system is how it responds to failure. Intuitively, for a grid amplifier we might expect each device to contribute equally to the radiated field, and the effect of a device failure should show up as a corresponding drop in the radiated field. Thus, a 10% failure rate would cause a 10% drop in the output field and a 1-dB drop in output power. Tests of grid amplifiers where devices have been randomly disabled have shown that the grid degrades gracefully as expected. This means that a grid amplifier could be much more reliable than a single high-power solid-state device or vacuum tube. This factor, in combination with the multimode behavior that preserves the propagation angles of beams, and the inherent low-loss of the quasi-optical coupling makes the grid amplifier an attractive alternative for amplifiers operating in the millimeter wavelengths.

8.6 QUASI-OPTICAL SYSTEMS

Amplifiers, oscillators, and mixers are just several of the components used in millimeter- and submillimeter-wave systems. Many other important system components, such as multipliers, filters, and phase shifters, can also be realized with quasi-optical grids. A common property of these grids is that their dynamic range increases in proportion to the number of devices in the array, yet noise performance is no worse than for circuits containing a single device.

To form a complete quasi-optical system, individual grid components need to be integrated. A heterodyne receiver, for example, consists of a mixer, a local oscillator, an amplifier, and filters. Figure 8.1 illustrates how a quasi-optical heterodyne receiver may be realized by cascading grids. An oscillator grid illuminates the mixer to provide a local oscillator. A grid amplifier, followed by a quasi-optical filter, is placed at the receiver input. Dielectric slabs can be included to provide input and output matching. Such a system is straightforward to build and does not require separate antennas that feed waveguide or transmission line circuits; all signal propagation occurs in free space.

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APPENDIX A

```
1  /***************************************************************************
2  *
3  *  Crossed Dipole Grid Impedance Calculator  V1.1
4  *
5  ***************************************************************************
6
7  This program computes Z11, Z1m, Zcm for a grid with unit cell width a,
8  unit cell height b, vertical lead thickness ws, horizontal lead thickness w,
9  substrate thickness d, and dielectric const Er, and lower vertical lead
10 length of s.  A mirror is assumed a distance l from the back of the
11 substrate.
12
13 Design data is input to the program through a configuration file
14 with the following format:
15
16
17 10.0e9    { fd Hz }     // design frequency
18 7.9       { a mm }      // x direction cell size (horiz) mm
19 7.9       { b mm }      // y direction cell size (vert) mm
20 0.5       { r }         // lower vert lead length / total vert cell length
21 0.5       { w mm }      // vertical lead width  mm
22 0.5       { ws mm }     // horizontal lead width mm
23 1.5875    { d mm }      // substrate thickness  mm
24 60.0      { l deg }       // distance mirror from substrate (deg)
25 2.2       { Er  }       // substrate dielectric constant
26 50        { Zo1 ohm }     // s-param normalizing impedance transistor side
27 377       { Zo2 ohm }     // s-param normalizing impedance free space side
28 40        { MM }        // number of terms in 'm' series
29 40        { NN }        // number of terms in 'n' series
30 0         { FLIP }      // 0 -> dielectric faces mirror (not implemented)
31 5         { START_FREQ GHz }
32 15        { STOP_FREQ GHz }
33 1         { INC_FREQ GHz }
34
35
```



```
36 This program has been tested with Borland Turbo C++ for DOS and OS/2.
37 */
38
39 #include <complex.h>
40 #include <conio.h>
41 #include <dos.h>
42 #include <io.h>
43 #include <stdio.h>
44 #include <stdlib.h>
45 #include <string.h>
46
47 #define sqr(x) ((x)*(x))
48 #define tiny 1.0e-20
49 #define PI 3.14159265358979324
50 #define TWOPI 6.28318530717958648
51 #define NONE 0
52 #define NO 0
53 #define YES 1
54
55 // fundamental constants
56 const double   mu = 1.2566e-9;          // H/mm
57 const double   Eo = 8.854e-15;          // F/mm
58 const double   Er_air = 1.0;
59 const double   c = 2.9979e11;           // mm/s
60 const double   Z_fs = 377.0;             // ohm
61
62 void ReadConfigDbl(double *x, FILE *config_file);
63 void ReadConfigInt(int *i, FILE *config_file);
64 double sinc(double x);
65 double kx(int m, double a);
66 double ky(int n, double b);
67 complex gamma(int m, int n, double er, double a, double b, double om);
68 complex zte(int m, int n, double er, double a, double b, double om);
69 complex ztm(int m, int n, double er, double a, double b, double om);
70 complex par(complex z1, complex z2);
71 complex ztran(complex zo, complex zl, complex g, double l);
72
73 void main(int argc, char *argv[])
74 {
75     complex z11, zcm, z1m, zteplu, ztmplu, zcalc, s11, s21;
76     int m, n, nn, deln;
77     int fields;
78     double kxt, kyt, f, om;
79     char scm_filename[81], slm_filename[81], s11_filename[81], z_filename[8
80     char rootname[81], l_filename[81], config_filename[81];
81     char *ch, input[81];
82     FILE *scm_file, *slm_file, *s11_file, *l_file, *z_file, *config_file;
83
84     // default design parameters
85     double   fd = 10e9;
86     double   a  = 8.6;          // x direction (horiz) mm
87     double   b  = a;            // y direction (vert) mm
88     double   r  = 0.5;          // lower vertical lead length / b
89     double   w  = 0.5;          // vertical lead width  mm
```

```
 90      double   ws = 0.5;         // horizontal lead width mm
 91      double   d  = 2.54;        // substrate thickness  mm
 92      double   arg_l = 45.0;     // distance mirror from substrate (deg)
 93      double   l = arg_l/360.0*c/fd;
 94      double   Er = 2.2;         // substrate diel const
 95      double   Zo1 = 50;         // norm impedance transistor side
 96      double   Zo2 = 377;        // norm impedance free space side
 97      int      MM = 40 ;
 98      int      NN = 40 ;
 99      int      FLIP = 0;                // 0 -> dielectric faces mirror
100      double   START_FREQ = 5;          // GHz
101      double   STOP_FREQ = 15;          // GHz
102      double   INC_FREQ = 10;           // GHz
103      strcpy(rootname, "xgrid");
104
105      /* say hello */
106
107      printf("\n\nCrossed Dipole Grid Analysis Version 1.1 \n");
108      printf("Copyright (C) Robert Weikle, Jon Hacker 1992\n\n");
109
110      // load in parameter file
111
112      if (argc ==2)
113      {
114          strcpy(rootname, argv[1]);
115          rootname[6] = '\0';                // max length is 6 chars
116          ch = strstr(rootname, ".");        // no dots allowed
117          if (ch != NULL)
118             *ch = '\0';
119      }
120      strcpy(config_filename, rootname);
121      strcat(config_filename, ".cfg");
122      config_file = fopen(config_filename, "r");
123      if (config_file == NULL)
124          printf("\nI can't find %s... using default parameters\n",
125            config_filename);
126      else
127      {
128          printf("\nreading parameters from %s... \n", config_filename);
129
130          ReadConfigDbl(&fd, config_file);
131          ReadConfigDbl(&a, config_file);
132          ReadConfigDbl(&b, config_file);
133          ReadConfigDbl(&r, config_file);
134          ReadConfigDbl(&w, config_file);
135          ReadConfigDbl(&ws, config_file);
136          ReadConfigDbl(&d, config_file);
137          ReadConfigDbl(&arg_l, config_file);
138          ReadConfigDbl(&Er, config_file);
139          ReadConfigDbl(&Zo1, config_file);
140          ReadConfigDbl(&Zo2, config_file);
141          ReadConfigInt(&MM, config_file);
142          ReadConfigInt(&NN, config_file);
```



```
143          ReadConfigInt(&FLIP, config_file);
144          ReadConfigDbl(&START_FREQ, config_file);
145          ReadConfigDbl(&STOP_FREQ, config_file);
146          ReadConfigDbl(&INC_FREQ, config_file);
147      }
148
149      l = arg_l / 360. * c / fd;
150
151      printf("fd = %6.4lf GHz\n", fd/1e9);
152      printf("a = %3.3lf mm\n", a);
153      printf("b = %3.3lf mm\n", b);
154      printf("r = %3.3lf (r = c/b) \n", r);
155      printf("w = %3.3lf mm\n", w);
156      printf("ws = %3.3lf mm\n", ws);
157      printf("d = %3.3lf mm\n", d);
158      printf("l =  %3.3lf mm (%2.1lf)\n", l, arg_l);
159      printf("Er = %3.2lf\n", Er);
160      printf("Zo1 = %3.2lf\n", Zo1);
161      printf("Zo2 = %3.2lf\n", Zo2);
162      printf("MM = %d   NN = %d\n", MM, NN);
163      printf("FLIP = %d  (0 -> substrate faces mirror) **Not Implemented \n",
164        FLIP);
165      printf("start frequency = %6.4lf GHz\n", START_FREQ);
166      printf("stop frequency = %6.4lf GHz\n", STOP_FREQ);
167      printf("frequency increment = %6.4lf GHz\n\n", INC_FREQ);
168
169      strcpy(slm_filename, rootname);
170      strcat(slm_filename, "lm.dev");
171      printf("file name for centre lead inductance (Lm) device file? (%s) ",
172        slm_filename);
173      gets(input);
174      if (input[0] != '\0')
175          strcpy(slm_filename, input);
176      slm_filename[12] = '\0';            // max length is 12 chars
177      slm_file = fopen(slm_filename, "w");
178      if (slm_file == NULL)
179      {
180          printf("\nI can't open '%s'... ", slm_filename);
181          printf("I'm quitting!\n");
182          exit(0);
183      }
184
185      strcpy(scm_filename, rootname);
186      strcat(scm_filename, "cm.dev");
187      printf("file name for centre lead capacitance (Cm) device file? (%s) ",
188        scm_filename);
189      gets(input);
190      if (input[0] != '\0')
191          strcpy(scm_filename, input);
192      scm_filename[12] = '\0';            // max length is 12 chars
193      scm_file = fopen(scm_filename, "w");
194      if (scm_file == NULL)
195      {
196          printf("\nI can't open '%s'... ", scm_filename);
```

```
197         printf("I'm quitting!\n");
198         exit(0);
199     }
200
201     strcpy(sll_filename, rootname);
202     strcat(sll_filename, "ll.dev");
203     printf("file name for lead inductance (L1) device file? (%s) ",
204       sll_filename);
205     gets(input);
206     if (input[0] != '\0')
207         strcpy(sll_filename, input);
208     sll_filename[12] = '\0';            // max length is 12 chars
209     sll_file = fopen(sll_filename, "w");
210     if (sll_file == NULL)
211     {
212         printf("\nI can't open '%s'... ", sll_filename);
213         printf("I'm quitting!\n");
214         exit(0);
215     }
216
217     strcpy(l_filename, rootname);
218     strcat(l_filename, ".lmp");
219     printf("output file name for lumped values file? (%s) ", l_filename);
220     gets(input);
221     if (input[0] != '\0')
222         strcpy(l_filename, input);
223     l_filename[12] = '\0';            // max length is 12 chars
224     l_file = fopen(l_filename, "w");
225     if (l_file == NULL)
226     {
227         printf("\nI can't open '%s'... ", l_filename);
228         printf("I'm quitting!\n");
229         exit(0);
230     }
231
232     strcpy(z_filename, rootname);
233     strcat(z_filename, ".z");
234     printf("output file name for impedance values file? (%s) ", z_filename);
235     gets(input);
236     if (input[0] != '\0')
237         strcpy(z_filename, input);
238     z_filename[12] = '\0';            // max length is 12 chars
239     z_file = fopen(z_filename, "w");
240     if (z_file == NULL)
241     {
242         printf("\nI can't open '%s'... ", z_filename);
243         printf("I'm quitting!\n");
244         exit(0);
245     }
246
247     clrscr();
248     printf("XDipole:\n");
249     printf("f (GHz)       Zlm (ohm)       Zcm (ohm)         Zll (ohm)\n\n");
```



```
250
251     fprintf(l_file, "{ Xdipole: a=%3.3lfmm b=%3.3lfmm r=%3.3lf w=%3.3lfmm",
252       a, b, r, w);
253     fprintf(l_file, " ws=%3.3lfmm d=%3.3lfmm Er=%2.1lf l=%2.1lfdeg }\n",
254       ws, d, Er, arg_l);
255     fprintf(l_file, "{ Zo1=%3.1lfohm  Zo2=%3.1lfohm  MM=%d, NN=%d }\n",
256       Zo1, Zo2, MM, NN );
257     fprintf(l_file, " f (GHz)    Lm (pH)         Cm (fF)     L (pH) \n\n");
258
259     fprintf(z_file, "{ Xdipole: a=%3.3lfmm b=%3.3lfmm r=%3.3lf w=%3.3lfmm",
260       a, b, r, w);
261     fprintf(z_file, " ws=%3.3lfmm d=%3.3lfmm Er=%2.1lf l=%2.1lfdeg }\n",
262       ws, d, Er, arg_l);
263     fprintf(z_file, "{ Zo1=%3.1lfohm Zo2=%3.1lfohm MM=%d, NN=%d }\n",
264       Zo1, Zo2, MM, NN );
265     fprintf(z_file, "  f (GHz)   Z (ohm)    Zc (ohm)   Zl (ohm)\n\n");
266
267     fprintf(scm_file, "{ Xdipole: a=%3.3lfmm b=%3.3lfmm r=%3.3lf w=%3.3lfmm",
268       a, b, r, w);
269     fprintf(scm_file, " ws=%3.3lfmm d=%3.3lfmm Er=%2.1lf l=%2.1lfdeg }\n",
270       ws, d, Er, arg_l);
271     fprintf(scm_file, "{ Zo1=%3.1lfohm MM=%d, NN=%d }\n",
272       Zo1, MM, NN);
273     fprintf(scm_file, "f\t s11\t s21\t s12\t s22 \n");
274
275     fprintf(slm_file, "{ Xdipole: a=%3.3lfmm b=%3.3lfmm r=%3.3lf w=%3.3lfmm",
276       a, b, r, w);
277     fprintf(slm_file, " ws=%3.3lfmm d=%3.3lfmm Er=%2.1lf l=%2.1lfdeg }\n",
278       ws, d, Er, arg_l);
279     fprintf(slm_file, "{ Zo1=%3.1lfohm MM=%d, NN=%d }\n",
280       Zo1, MM, NN);
281     fprintf(slm_file, "f\t s11\t s21\t s12\t s22 \n");
282
283     fprintf(sll_file, "{ Xdipole: a=%3.3lfmm b=%3.3lfmm r=%3.3lf w=%3.3lfmm",
284       a, b, r, w);
285     fprintf(sll_file, " ws=%3.3lfmm d=%3.3lfmm Er=%2.1lf l=%2.1lfdeg }\n",
286       ws, d, Er, arg_l);
287     fprintf(sll_file, "{ Zo2=%3.1lfohm MM=%d, NN=%d }\n",
288       Zo2, MM, NN);
289     fprintf(sll_file, "f\t s11\t s21\t s12\t s22 \n");
290
291     for (f=START_FREQ; f <= STOP_FREQ; f += INC_FREQ)
292     {
293         om=2*PI*1e9*f;
294
295         zll=0;
296         zcm=0;
297
298         for (m=2; m<=MM; m+=2)
299         {
300 // compute Zte+ ('+' direction is looking to the short behind the grid)
301
302 // First, compute the impedance at the back of the substrate looking towards
```

```
303 // the short a distance l away in air
304         zteplu = ztran(zte(m,0,1,a,b,om), 0, gamma(m,0,1,a,b,om), 1);
305
306 // now compute the impedance at the front of the grid looking back at the
307 // mirror through the substrate of thickness d
308         zteplu = ztran(zte(m,0,Er,a,b,om), zteplu, gamma(m,0,Er,a,b,om),d)
309
310 // now add the term to the L1 summation
311         zl1 += (2*b/a)*sqr(sinc(m*PI*w/(2*a)))*par(zte(m,0,1,a,b,om),
312                 zteplu);
313     }
314
315 // only sum 'n odd' modes if r = 0.5
316     if (r == 0.5)
317         deln = 2;
318     else
319         deln = 1;
320
321     for (n=1; n<=NN; n+=deln)
322     {
323         ztmplu = ztran(ztm(0,n,1,a,b,om), 0, gamma(0,n,1,a,b,om), 1);
324         ztmplu = ztran(ztm(0,n,Er,a,b,om), ztmplu, gamma(0,n,Er,a,b,om),d)
325         zcalc = par(ztm(0,n,1,a,b,om),ztmplu);
326         zcalc *= sqr(sin(n*PI*r)*sinc(n*PI*ws/(2*b))/ky(n, b));
327         zcm += (2*zcalc/(a*b));
328     }
329
330     zlm=0;
331
332     for (n=1; n<=NN; n+=deln)
333         for (m=2; m<=MM; m+=2)
334         {
335             kxt=kx(m, a);
336             kyt=ky(n, b);
337
338             zteplu = ztran(zte(m,n,1,a,b,om),0, gamma(m,n,1,a,b,om),1);
339             zteplu = ztran(zte(m,n,Er,a,b,om), zteplu,
340                     gamma(m,n,Er,a,b,om), d);
341
342             ztmplu = ztran(ztm(m,n,1,a,b,om), 0, gamma(m,n,1,a,b,om), 1);
343             ztmplu = ztran(ztm(m,n,Er,a,b,om), ztmplu,
344                     gamma(m,n,Er,a,b,om), d);
345
346             zcalc = sqr((kxt/kyt)+(kyt*a/(kxt*(a-w))))
347                 *par(zteplu,zte(m,n,1,a,b,om));
348             zcalc += sqr(1-(a/(a-w)))*par(ztmplu,ztm(m,n,1, a, b, om));
349             zcalc *= sqr(sin(n*PI*r)*sinc(m*PI*w/(2*a))
350                     *sinc(n*PI*ws/(2*b)));
351             zcalc /= (sqr(kxt)+sqr(kyt));
352
353             zlm += 4*zcalc/(a*b);
354         }
355     printf("%3.1lf \t %4.3lf", f, real(zlm));
```



```
356         if (imag(zlm) < 0)
357             printf("-j%4.3lf    %4.3lf", -imag(zlm), real(zcm));
358         else
359             printf("+j%4.3lf    %4.3lf", imag(zlm), real(zcm));
360         if (imag(zcm) < 0)
361             printf("-j%4.3lf    %4.3lf", -imag(zcm), real(zl1));
362         else
363             printf("+j%4.3lf    %4.3lf", imag(zcm), real(zl1));
364         if (imag(zl1) < 0)
365             printf("-j%4.3lf \n", -imag(zl1));
366         else
367             printf("+j%4.3lf \n", imag(zl1));
368
369         fprintf(z_file, "%3.1lf \t %4.3lf", f, real(zlm));
370         if (imag(zlm) < 0)
371             fprintf(z_file, "-j%4.3lf    %4.3lf", -imag(zlm), real(zcm));
372         else
373             fprintf(z_file, "+j%4.3lf    %4.3lf", imag(zlm), real(zcm));
374         if (imag(zcm) < 0)
375             fprintf(z_file, "-j%4.3lf    %4.3lf", -imag(zcm), real(zl1));
376         else
377             fprintf(z_file, "+j%4.3lf    %4.3lf", imag(zcm), real(zl1));
378         if (imag(zl1) < 0)
379             fprintf(z_file, "-j%4.3lf \n", -imag(zl1));
380         else
381             fprintf(z_file, "+j%4.3lf \n", imag(zl1));
382
383 // compute centre capacitance (Cm) s-parameters
384         s11 = (zcm)/(zcm+2*Zo1);
385         s21 = (2*Zo1)/(zcm+2*Zo1);
386
387         fprintf(scm_file, "%4.2lf  %7.6lf %4.3lf  %7.6lf %4.3lf ",
388           f, abs(s11), arg(s11)*180/PI, abs(s21), arg(s21)*180/PI);
389         fprintf(scm_file, " %7.6lf %4.3lf  %7.6lf %4.3lf \n",
390           abs(s21), arg(s21)*180/PI, abs(s11), arg(s11)*180/PI);
391
392 // compute centre inductance (Lm) s-parameters
393         s11 = (zlm)/(zlm+2*Zo1);
394         s21 = (2*Zo1)/(zlm+2*Zo1);
395
396
397         fprintf(slm_file, "%4.2lf  %7.6lf %4.3lf  %7.6lf %4.3lf ",
398           f, abs(s11), arg(s11)*180/PI, abs(s21), arg(s21)*180/PI);
399         fprintf(slm_file, " %7.6lf %4.3lf  %7.6lf %4.3lf \n",
400           abs(s21), arg(s21)*180/PI, abs(s11), arg(s11)*180/PI);
401
402
403 //  note that Z11 is the inductance on the free space side of the transformer
404 //  and needs to be halved for transistor side value (we will generate
405 //  s-parameters for free-space side here)
406
407         s11 = (zl1)/(zl1+2*Zo2);
408         s21 = (2*Zo2)/(zl1+2*Zo2);
```

```
409
410         fprintf(sll_file, "%4.2lf  %7.6lf %4.3lf  %7.6lf %4.3lf ",
411           f, abs(s11), arg(s11)*180/PI, abs(s21), arg(s21)*180/PI);
412         fprintf(sll_file, " %7.6lf %4.3lf  %7.6lf %4.3lf \n",
413           abs(s21), arg(s21)*180/PI, abs(s11), arg(s11)*180/PI);
414
415         fprintf(l_file, "%4.2lf     %4.3lf     %4.3lf     %4.3lf  ",
416           f, imag(zlm)/2/PI/f*1e3, -1/imag(zcm)/2/PI/f*1e6,
417           imag(zll)/2/PI/f*1e3);
418         if ( fabs(real(zlm)) >= 1e-6 ||  fabs(real(zcm)) >= 1e-6
419             || fabs(real(zll)) >= 1e-6)
420             fprintf(l_file, " ****   not pure reactance ***\n");
421         else
422             fprintf(l_file, " \n");
423     }
424 }
425
426
427 /******************************************************************
428     ReadConfigDbl()
429
430     reads double from config_file,  aborts on error
431
432 ******************************************************************/
433 void ReadConfigDbl(double *x, FILE *config_file)
434 {
435     int fields;
436     char input[256];
437
438     if (fgets(input, 255, config_file) == NULL)
439     {
440         printf("\nConfig file unreadable... I quit.\n");
441         printf("\n -> Input Stream: %s\n\n", input);
442         exit(0);
443     }
444     fields = sscanf(input, "%lf", x);
445
446     if (fields != 1)
447     {
448         printf("\nConfig file unreadable... I quit.\n\n");
449         printf("\n -> Input Stream: %s\n\n", input);
450         exit(0);
451     }
452 }
453
454
455 /******************************************************************
456     ReadConfigInt()
457
458     reads integer from config_file,  aborts on error
459
460 ******************************************************************/
461 void ReadConfigInt(int *i, FILE *config_file)
```



```
462 {
463     int fields;
464     char input[256];
465
466     if (fgets(input, 255, config_file) == NULL)
467     {
468         printf("\nConfig file unreadable... I quit.\n");
469         printf("\n -> Input Stream: %s\n\n", input);
470         exit(0);
471     }
472     fields = sscanf(input, "%d", i);
473
474     if (fields != 1)
475     {
476         printf("\nConfig file unreadable... I quit.\n\n");
477         printf("\n -> Input Stream: %s\n\n", input);
478         exit(0);
479     }
480 }
481
482
483 /******************************************************************
484     sinc()
485
486 ******************************************************************/
487 double sinc(double x)
488 {
489     if (x == 0)
490         return (1.0);
491     else
492         return (sin(x)/x);
493 }
494
495
496 /******************************************************************
497     kx()
498
499 ******************************************************************/
500 double kx(int m, double a)
501 {
502     return (m*PI/a);
503 }
504
505
506 /******************************************************************
507     ky()
508
509 ******************************************************************/
510 double ky(int n, double b)
511 {
512     return (n*PI/b);
513 }
514
```

```
515
516 /*****************************************************************
517      gamma()
518
519 *****************************************************************/
520 complex gamma(int m, int n, double er, double a, double b, double om)
521 {
522       return (sqrt(complex(sqr(kx(m, a))+sqr(ky(n, b))-sqr(om)*mu*Eo*er, 0)));
523 }
524
525
526 /*****************************************************************
527      zte()
528
529 *****************************************************************/
530 complex zte(int m, int n, double er, double a, double b, double om)
531 {
532      return (om*mu/(complex(0, -1.) * gamma(m, n, er, a, b, om)));
533 }
534
535
536 /*****************************************************************
537      ztm()
538
539 *****************************************************************/
540 complex ztm(int m, int n, double er, double a, double b, double om)
541 {
542      if (om*er == 0)
543          return (1e9);
544      else
545          return (complex(0, -1.0) * gamma(m, n, er, a, b, om)/(om*Eo*er));
546 }
547
548
549 /*****************************************************************
550      par()
551
552 *****************************************************************/
553 complex par(complex z1, complex z2)
554 {
555      complex ztemp=z1+z2;
556
557 // check for parallel resonance
558      if (abs(ztemp) == 0)
559          return (1e9);
560      else
561          return (z1 *z2 /(ztemp));
562 }
563
564
565 /*****************************************************************
566      ztran()
567
```



```
568 *****************************************************************/
569 complex ztran(complex zo, complex zl, complex g, double l)
570 {
571      complex ztemp;
572
573      if (real(g*l) > 20)
574          return (zo);
575      else
576      {
577          ztemp = zo+(zl*tanh(g*l));
578 // check for open cct case
579          if ( abs(ztemp) == 0 )
580              return (1e9);
581          else
582              return (zo*(zl+(zo*tanh(g*l)))/ztemp);
583      }
584 }
```

APPENDIX B

```
1 /**************************************************************************
2 *
3 *  Bow-tie Grid Impedance Calculator V1.0
4 *
5 **************************************************************************
6
7 This program computes Z_bt and Theta_bt for a grid with unit cell
8 width 2d, 45 degree bow angle, substrate thickness t, and dielectric
9 const Er.  A mirror is assumed a distance l from the back of the
10 substrate.
11
12 Design data is input to the program through the configuration file
13 bowtie.cfg with the following format:
14
15 377.0 { Zd  ohm }          // s-parameter normalizing impedance
16 10e9  { fd  Hz }           // design frequency
17 10.5  { Er_subs }          // substrate
18 20    { l  degrees }       // air gap between mirror and substrate
19 0.635  { t mm }            // substrate thickness
20 3.1   { d  mm }            // bowtie half cell width
21 20    { MM }               // number of 'x' terms in series approx.
22 20    { NN }               // number of 'y' terms in series approx.
23 0     { FLIP }             // 0 -> substrate faces mirror
24 45    { ang  degrees }     // bowtie angle (only valid for 45deg)
25 5.0    { START_FREQ GHz }
26 15.0    { STOP_FREQ GHz }
27 1.0   { INC_FREQ  GHz }
28 bow.cof                    // default coefficient file name
29
30 This program has been tested with Borland Turbo C++ for DOS and OS/2.
31 */
32
33 #include <complex.h>
```

```
34 #include <conio.h>
35 #include <dos.h>
36 #include <io.h>
37 #include <stdio.h>
38 #include <stdlib.h>
39 #include <string.h>
40
41 #define sqr(x) ((x)*(x))
42 #define tiny 1.0e-20
43 #define PI 3.14159265358979324
44 #define TWOPI 6.28318530717958648
45 #define NONE 0
46 #define NO 0
47 #define YES 1
48
49 // fundamental constants
50 const double   mu = 1.2566e-9;        // H/mm
51 const double   Eo = 8.854e-15;        // F/mm
52 const double   Er_air = 1.0;
53 const double   v = 2.9979e11;         // mm/s
54 const double   Z_fs = 377.0;          // ohm
55
56 double C[51][51];      // something larger than necessary
57
58 void ReadConfigDbl(double *x, FILE *config_file);
59 void ReadConfigInt(int *i, FILE *config_file);
60 double K(double x, double y);
61 void trapK(double a, double b, double *s, int n, double psi);
62 void simpK(double a,double b, double *s, double psi);
63 double fmn(double x, double y, double z);
64 void trapf(double a, double b, double y, double *s, int n, double psi);
65 void simpf(double a,double b, double x, double *s, double psi);
66 double Amn(int x, int y, double z, int flag, double d, double psi);
67 void trapa(double a, double b, int y, int z, double *s, int n, double d,
68            double psi, int flag);
69 void simpa(double a, double b, int x, int y, double *s, int flag,
70            double d, double psi);
71 void coeff(FILE *coeff_file, int read_coeff, double ang,
72            double d, double psi, int MM, int NN );
73 int ep(int x, int y);
74 complex xtanh(complex x);
75 complex z_te(complex gamma, double w);
76 complex z_tm(complex gamma, double w, double er);
77 complex propagate(double w, double er, double d, int m, int n);
78 void imp_neg(double w, double Er_subs, double d, double t, double l,
79              int FLIP, int m, int n, complex *zn_te, complex *zn_tm);
80 void imp_plus(double w, double Er_subs, double d, double t, int FLIP,
81               int m, int n, complex *zp_te, complex *zp_tm);
82 void sumterms(double w, double Er_subs, double d, double t, double l,
83               int FLIP, int MM, int NN, complex *zl, complex *yc,
84               complex *ytem);
85
86 int main(int argc, char *argv[])
```



```
87 {
88     int status, fields, read_coeff, file_MM, file_NN;
89     double file_d, file_ang, Zo, Lo, arg_l, psi, freq;
90     complex s11, s21, s12, s22, z, y, gam, zl, yc, ytem;
91     char    s_filename[81], coeff_filename[81], config_filename[81],
92             l_filename[81], input[81], *ch, rootname[81];
93     FILE    *s_file, *coeff_file, *l_file, *config_file;
94
95 // default design parameters
96     double  Zd = 50.0;              // ohm
97     double  fd = 10e9;              // Hz
98     double  Er_subs = 10.2;         //
99     double  l = 7.5;                // mm   (air gap)
100    double  t = 2.54;               // mm   (substrate thickness)
101    double  d = 2.5;                // mm   (half cell width)
102    int     MM = 20;                // no. terms included in series
103    int     NN = 20;                // no. terms included in series
104    int     FLIP = 1;               // 0 -> dielectric faces mirror
105    double  ang = 45;               // degrees (must be 45deg)
106    double  START_FREQ = 5;         // GHz
107    double  STOP_FREQ = 15;         // GHz
108    double  INC_FREQ = 0.5;         // GHz
109    strcpy(rootname, "bowtie");
110
111    /* say hello */
112    printf("\n\nBowtie Impedance Calculator Version 1.0\n");
113    printf("Copyright (C) Robert Weikle, Jon Hacker 1991\n\n");
114
115    // load in parameter file
116
117    if (argc !=2 )
118    {
119       printf("usage: bowtie config_filename\n");
120       exit(1);
121    }
122    else
123    {
124       strcpy(rootname, argv[1]);
125       rootname[8] = '\0';                // max length is 8 chars
126       ch = strstr(rootname, ".");         // no dots allowed
127       if (ch != NULL)
128          *ch = '\0';
129    }
130    strcpy(config_filename, rootname);
131    strcat(config_filename, ".cfg");
132    config_file = fopen(config_filename, "r");
133    if (config_file == NULL)
134       printf("\nI can't find %s... using default parameters\n",
135          config_filename);
136    else
137    {
138       printf("\nreading parameters from %s... \n", config_filename);
139       ReadConfigDbl(&Zd, config_file);
140       ReadConfigDbl(&fd, config_file);
```

```
141         ReadConfigDbl(&Er_subs, config_file);
142         ReadConfigDbl(&arg_l, config_file);
143         ReadConfigDbl(&t, config_file);
144         ReadConfigDbl(&d, config_file);
145         ReadConfigInt(&MM, config_file);
146         ReadConfigInt(&NN, config_file);
147         ReadConfigInt(&FLIP, config_file);
148         ReadConfigDbl(&ang, config_file);
149         if (ang!=45.0)
150         {
151             printf("\nError: bowtie angle must be 45 degrees\n");
152             exit(1);
153         }
154         ReadConfigDbl(&START_FREQ, config_file);
155         ReadConfigDbl(&STOP_FREQ, config_file);
156         ReadConfigDbl(&INC_FREQ, config_file);
157
158         if (fgets(input, 81, config_file) == NULL)
159         {
160             printf("\nConfig file unreadable... I quit.\n\n");
161             exit(0);
162         }
163         ch = strchr(input, '\n');
164         if (ch != NULL)
165             *ch = '\0';                     // remove linefeed
166         strcpy(coeff_filename, input);
167     }
168
169     l = arg_l / 360. * v / fd;
170     psi = ang*PI/180;
171
172     printf("\nZd = %2.1lf ohm\n", Zd);
173     printf("fd = %6.4lf GHz\n", fd/1e9);
174     printf("Er_subs = %3.2lf\n", Er_subs);
175     printf("l =  %3.2lf mm (%2.1lfdeg)\n", l, arg_l);
176     printf("t = %3.2lf mm\n", t);
177     printf("d = %3.2lf mm\n", d);
178     printf("MM = %d   NN = %d\n", MM, NN);
179     printf("FLIP = %d  (0 -> substrate faces mirror) \n", FLIP);
180     printf("psi = %2.1lfdeg \n", ang);
181     printf("start frequency = %6.4lf GHz\n", START_FREQ);
182     printf("stop frequency = %6.4lf GHz\n", STOP_FREQ);
183     printf("frequency increment = %6.4lf GHz\n", INC_FREQ);
184
185     printf("\nDo you want to read in a coefficient file (y/n)?");
186     status = 1;
187     while(status)
188     {
189         *ch = getch();
190         if (*ch == 'Y' || *ch == 'N'  || *ch == 'y' || *ch == 'n')
191             status = 0;
192     }
193     if( *ch == 'Y' || *ch == 'y' )
```



```
194     {
195         printf("y\n\n");
196         read_coeff = YES;
197         printf("I need a coefficient file for:\n");
198         printf("d=%3.2lfmm, bow=%2.1lfdeg, MM=%d, NN=%d\n\n",
199           d, ang, MM, NN);
200         printf("filename? (%s) ", coeff_filename);
201         gets(input);
202         if (input[0] != '\0')
203             strcpy(coeff_filename, input);
204         coeff_filename[12] = '\0';           // max length is 12 chars
205         coeff_file = fopen(coeff_filename, "r");
206         if (coeff_file == NULL)
207         {
208             printf("\nI can't open '%s'... ", coeff_filename);
209             printf("I'm quitting!\n");
210             exit(0);
211         }
212         fgets(input, 81, coeff_file);
213         fgets(input, 81, coeff_file);
214         fields = sscanf(input, "%lf %lf %d %d", &file_d,
215           &file_ang, &file_MM, &file_NN);
216         if( d!=file_d || ang!=file_ang || MM!=file_MM
217           || NN!=file_NN || fields != 4)
218         {
219             printf("\nI don't think '%s' contains the right coefficients... ",
220               coeff_filename);
221             printf("I'm quitting!\n");
222             exit(0);
223         }
224     }
225     else
226     {
227         printf("n\n\n");
228         read_coeff = NO;
229         printf("output filename for coefficient data? (%s) ", coeff_filename);
230         gets(input);
231         if (input[0] != '\0')
232             strcpy(coeff_filename, input);
233         coeff_filename[12] = '\0';           // max length is 12 chars
234         coeff_file = fopen(coeff_filename, "w");
235         if (coeff_file == NULL)
236         {
237             printf("\nI can't open '%s'... ", coeff_filename);
238             printf("I'm quitting!\n");
239             exit(0);
240         }
241     }
242
243     strcpy(s_filename, rootname);
244     strcat(s_filename, ".dev");
245     printf("\noutput file name for s-parameter device file? (%s) ",
246           s_filename);
```

```
247     gets(input);
248     if (input[0] != '\0')
249         strcpy(s_filename, input);
250     s_filename[12] = '\0';            // max length is 12 chars
251     s_file = fopen(s_filename, "w");
252     if (s_file == NULL)
253     {
254         printf("\nI can't open '%s'... ", coeff_filename);
255         printf("I'm quitting!\n");
256         exit(0);
257     }
258
259     strcpy(l_filename, rootname);
260     strcat(l_filename, ".lmp");
261     printf("\noutput file name for lumped element file? (%s) ", l_filename);
262     gets(input);
263     if (input[0] != '\0')
264         strcpy(l_filename, input);
265     l_filename[12] = '\0';            // max length is 12 chars
266     l_file = fopen(l_filename, "w");
267     if (l_file == NULL)
268     {
269         printf("\nI can't open '%s'... ", l_filename);
270         printf("I'm quitting!\n");
271         exit(0);
272     }
273     coeff(coeff_file, read_coeff, ang, d, psi, MM, NN);
274     clrscr();
275     printf("\t f (GHz)     Zo (ohm)         Lo (deg)\n\n");
276     fprintf(l_file, "{ Bowtie: d=%3.2lfmm, bow=%2.1lfdeg, MM=%d, NN=%d ",
277       d, ang, MM, NN);
278     fprintf(l_file, "t=%3.2lf l=%3.2lf Er=%2.1lf Zd=%3.1lf}\n",
279       t, l, Er_subs, Zd);
280
281     fprintf(l_file, " f (GHz)     Zo (ohm)         Lo (deg)\n\n");
282
283     fprintf(s_file, "{ Bowtie: d=%3.2lfmm, bow=%2.1lfdeg, MM=%d, NN=%d ",
284       d, ang, MM, NN);
285     fprintf(s_file, "t=%3.2lf l=%3.2lf Er=%2.1lf Zd=%3.1lf}\n",
286       t, l, Er_subs, Zd);
287
288     fprintf(s_file, "f\t s11\t s21\t s12\t s22 \n");
289
290     for (freq=START_FREQ; freq<=STOP_FREQ; freq+=INC_FREQ)
291     {
292     // compute bowtie transmission line impedance and length
293         sumterms(2*PI*freq*1e9,Er_subs,d,t,l,FLIP,MM,NN,&zl,&yc,&ytem);
294         Zo = sqrt(fabs(imag(zl)/imag(yc)));
295         Lo = sqrt(fabs(imag(zl)*imag(yc)));
296
297     // compute s-parameters for equivalent transmission line
298         z = complex(Zo/Zd, 0);
299         y = 1/z;
```



```
300         gam = complex(0, Lo);
301         s11 = ((z-y)*sinh(gam)) /
302               (2*cosh(gam) + (z+y)*sinh(gam));
303         s22 = s11;
304         s21 = 2 / (2*cosh(gam) + (z+y)*sinh(gam));
305         s12 = s21;
306
307     // print out results
308         printf("\t %4.2lf\t   %7.4lf\t %7.4lf\t", freq, Zo, Lo*180/PI);
309         printf("\n");
310
311         fprintf(l_file, "%4.2lf\t   %7.4lf\t %7.4lf\n", freq, Zo, Lo*180/PI);
312
313         fprintf(s_file, "%5.4lf  %5.4lf  %5.2lf  ",
314           freq, sqrt(norm(s11)), arg(s11)*180/PI);
315         fprintf(s_file, "%5.4lf  %5.2lf  ", sqrt(norm(s21)), arg(s21)*180/PI);
316         fprintf(s_file, "%5.4lf  %5.2lf  ", sqrt(norm(s12)), arg(s12)*180/PI);
317         fprintf(s_file, "%5.4lf  %5.2lf \n", sqrt(norm(s22)), arg(s22)*180/PI);
318     }
319     fcloseall();
320     exit(0);
321 }
322
323 /******************************************************************
324     ReadConfigDbl()
325
326     reads double from config_file,  aborts on error
327
328 ******************************************************************/
329 void ReadConfigDbl(double *x, FILE *config_file)
330 {
331     int fields;
332     char input[256];
333
334     if (fgets(input, 255, config_file) == NULL)
335     {
336         printf("\nConfig file unreadable... I quit.\n");
337         printf("\n -> Input Stream: %s\n\n", input);
338         exit(0);
339     }
340     fields = sscanf(input, "%lf", x);
341
342     if (fields != 1)
343     {
344         printf("\nConfig file unreadable... I quit.\n\n");
345         printf("\n -> Input Stream: %s\n\n", input);
346         exit(0);
347     }
348 }
349
350
351 /******************************************************************
352     ReadConfigInt()
```

```
353
354     reads integer from config_file,  aborts on error
355
356 ******************************************************************/
357 void ReadConfigInt(int *i, FILE *config_file)
358 {
359     int fields;
360     char input[256];
361
362     if (fgets(input, 255, config_file) == NULL)
363     {
364         printf("\nConfig file unreadable... I quit.\n");
365         printf("\n -> Input Stream: %s\n\n", input);
366         exit(0);
367     }
368     fields = sscanf(input, "%d", i);
369
370     if (fields != 1)
371     {
372         printf("\nConfig file unreadable... I quit.\n\n");
373         printf("\n -> Input Stream: %s\n\n", input);
374         exit(0);
375     }
376 }
377
378 /*****************************************************************
379     K()
380
381 ******************************************************************/
382 double K(double x, double y)
383 {
384     return(2/sqrt((1+x)*(1-sqr(x*sin(y)))));
385 }
386
387 /*****************************************************************
388     trapK()
389
390 ******************************************************************/
391 void trapK(double a, double b, double *s, int n, double psi)
392 {
393     int j;
394     static int glitk=0;
395     double x, tnm, sum, del;
396
397     if (n == 1)
398     {
399         *s = 0.5*(b-a)*( K(1-sqr(a),psi) + K(1-sqr(b),psi));
400         glitk= 1;
401     }
402     else
403     {
404         tnm = glitk;
405         del = (b-a)/tnm;
```



```
406         x = a+0.5*del;
407         sum = 0.0;
408         for (j=1; j<=glitk; j++)
409         {
410             sum = sum+K(1-sqr(x),psi);
411             x = x + del;
412         }
413         *s = 0.5*(*s+(b-a)*sum/tnm);
414         glitk = 2*glitk;
415     }
416 }
417
418
419 /*****************************************************************
420     simpK()
421
422 ******************************************************************/
423 void simpK(double a, double b, double *s, double psi)
424 {
425
426 // constants...
427     const double   EPS=1e-6;
428     const int      JMAX = 20;
429
430 // variables...
431     int j;
432     double st, ost, os;
433     char input[81];
434
435     printf("\nintegrating normalizing value");
436     ost = -1e30;
437     os = -1e30;
438     for (j=1; j<=JMAX; j++)
439     {
440         printf(".");
441         trapK(a, b, &st, j, psi);
442         *s = (4*st-ost)/3;
443         if (fabs(*s-os) < EPS*fabs(os))
444         {
445             printf(" done\n\n");
446             return;                         // quit if within tolerance
447         }
448         os = *s;
449         ost = st;
450     }
451     printf("pause in SIMPK - too many steps \n");
452     gets(input);
453 }
454
455
456 /*****************************************************************
457     fmn()
458
```

```
459 ******************************************************************/
460 double fmn(double x, double y, double z)
461 {
462     double denom, num;
463
464     num = 2*cos(x*y*sin(z)/sqrt(1-sqr(y*sin(z))));
465     denom = sqrt((1-sqr(y*sin(z)))*(1+y));
466     return(num/denom);
467 }
468
469
470 /*****************************************************************
471     trapf()
472
473 *****************************************************************/
474 void trapf(double a, double b, double y, double *s, int n, double psi)
475 {
476     int j;
477     static int glitf=0;
478     double x, tnm, sum, del;
479
480     if (n == 1)
481     {
482         *s= 0.5*(b-a)*(fmn(y,1-sqr(a),psi) + fmn(y,1-sqr(b),psi));
483         glitf= 1;
484     }
485     else
486     {
487         tnm = glitf;
488         del = (b-a)/tnm;
489         x = a+0.5*del;
490         sum = 0.0;
491         for (j=1; j<=glitf; j++)
492         {
493             sum = sum+fmn(y,1-sqr(x),psi);
494             x = x+del;
495         }
496         *s = 0.5*(*s+(b-a)*sum/tnm);
497         glitf = 2*glitf;
498     }
499 }
500
501
502 /*****************************************************************
503     simpf()
504
505 *****************************************************************/
506 void simpf(double a,double b, double x, double *s, double psi)
507 {
508 //   const
509     const double   EPS=1e-5;
510     const int      JMAX = 40;
511
512 // var
```



```
513     int j;
514     double st, ost, os;
515     char input[81];
516
517     ost = -1e30;
518     os = -1e30;
519     for(j=1; j<= JMAX; j++)
520     {
521         trapf(a,b,x,&st,j,psi);
522         *s = (4*st-ost)/3;
523         if (fabs(*s-os) < EPS*fabs(os))
524             return;                          // quit if within tolerance
525         os = *s;
526         ost = st;
527     }
528     printf("pause in SIMPF - too many steps");
529     gets(input);
530 }
531
532
533 /*****************************************************************
534     Amn()
535
536 *****************************************************************/
537 double Amn(int x, int y, double z, int flag, double d, double psi)
538 {
539     double s;
540
541     if (flag == 0)
542         simpf(0, 1, x*PI*z/d, &s, psi);
543     else
544     {
545         s = 1/sqrt(2*x*z*tan(psi)/d);
546         s = s*cos(x*PI*z/d*tan(psi) -PI/4);
547     }
548     return( s*cos(y*PI*z/d) );
549 }
550
551
552 /*****************************************************************
553     trapa()
554
555 *****************************************************************/
556 void trapa(double a, double b, int y, int z, double *s, int n,
557         double d, double psi, int flag)
558 {
559     int j;
560     static int glita=0;
561     double  x, tnm, sum, del;
562
563     if (n == 1)
564     {
565         *s= 0.5*(b-a)*(Amn(y,z,a,flag,d,psi) + Amn(y,z,b,flag,d,psi));
```

```
566             glita= 1;
567         }
568         else
569         {
570             tnm = glita;
571             del = (b-a)/tnm;
572             x = a+0.5*del;
573             sum = 0.0;
574             for(j=1; j<=glita; j++)
575             {
576                 sum = sum+Amn(y,z,x,flag,d,psi);
577                 x = x+del;
578             }
579             *s = 0.5*(*s+(b-a)*sum/tnm);
580             glita = 2*glita;
581         }
582 }
583
584
585 /*****************************************************************
586         simpa()
587
588 *****************************************************************/
589 void simpa(double a, double b, int x, int y, double *s, int flag,
590             double d, double psi)
591 {
592 // constants...
593     const double    EPS=1e-5;
594     const int       JMAX = 40;
595
596 // variables...
597     int j;
598     double st, ost, os;
599     char input[81];
600
601     ost = -1e30;
602     os = -1e30;
603     for(j=1; j<=JMAX; j++)
604     {
605         trapa(a,b,x,y,&st,j,d,psi,flag);
606         *s = (4*st-ost)/3;
607         if (fabs(*s-os) < EPS*fabs(os))
608             return;                              // quit if within tolerance
609         os = *s;
610         ost = st;
611     }
612     printf("pause in SIMPA - too many steps \n");
613     gets(input);
614 }
615
616
617 /*****************************************************************
618     coeff()
```



```
619
620 *****************************************************************/
621 void coeff(FILE *coeff_file, int read_coeff, double ang,
622             double d, double psi, int MM, int NN)
623 {
624     int m, n, flag;
625     double int1, int2, temp;
626
627     if (read_coeff == YES)
628     {
629         for(n=0; n<=NN; n++)
630         {
631             for(m=0; m<=MM; m++)
632             {
633                 fscanf(coeff_file, "%lf \n", &C[m][n]);
634             }
635         }
636     }
637     else
638     {
639         fprintf(coeff_file, "d=%3.2lfmm, bow=%2.1lfdeg, MM=%d, NN=%d\n",
640           d, ang, MM, NN);
641         fprintf(coeff_file, "%5.4lf \t %5.4lf \t %d \t %d \n",
642           d, ang, MM, NN);
643
644         simpK(0, 1, &int1, psi);
645         printf("integrating coefficients... \n\n");
646         for(n=0; n<=NN; n++)
647         {
648             for(m=0; m<=MM; m++)
649             {
650                 if (m > 0)
651                 {
652                     flag = 0;
653                     simpa(0, 2*d/m/PI, m, n, &temp, flag, d, psi);
654                     flag = 1;
655                     simpa(2*d/m/PI, d, m, n, &int2, flag, d, psi);
656                     int2 = int2+temp;
657                     C[m][n] = int2/int1/d;
658                 }
659                 else if (n > 0)
660                     C[m][n] = 0;
661                 else
662                 {
663                     flag = 0;
664                     simpa(0, d, m, n, &int2, flag, d, psi);
665                     C[m][n] = int2/int1/d;
666                 }
667                 printf("A[%d,%d] = B[%d,%d] = %8.7lf \n",
668                   m, n, n, m, C[m][n]);
669                 fprintf(coeff_file, "%8.7lf \n", C[m][n]);
670             }
671         }
```

```
672     fclose(coeff_file);
673     printf("\n done \n\n");
674     }
675 }
676
677
678 /*****************************************************************
679     ep()
680
681 *****************************************************************/
682 int ep(int m, int n)
683 {
684     if (m == n)
685         return(1);
686     else
687         return(2);
688 }
689
690
691 /*****************************************************************
692     xtanh()
693     checks for a large real argument and returns 1 to avoid an
694     overflow
695 *****************************************************************/
696 complex xtanh(complex x)
697 {
698     complex y;
699
700     if (real(x) > 100.)
701     {
702         if (real(x)*imag(x) != 0.0)
703             printf("\nxtanh(): arg x  must be pure real if real(x) > 100 \n");
704         return (1.0000000);
705     }
706     else
707     {
708         y = tanh(x);
709         return (y);
710     }
711 }
712
713
714 /*****************************************************************
715     z_te()
716
717 *****************************************************************/
718 complex  z_te(complex gamma, double w)
719 {
720     complex j = complex(0,1), z_te;
721
722     z_te = j * w * mu / gamma;
723     return( z_te );
724 }
```



```
725
726
727 /*****************************************************************
728     z_tm()
729
730 *****************************************************************/
731 complex z_tm(complex gamma, double w, double er)
732 {
733     complex j = complex(0,1), z_tm;
734
735     z_tm = gamma / (j * w * Eo * er);
736     return( z_tm );
737 }
738
739
740 /*****************************************************************
741     propagate()
742
743 *****************************************************************/
744 complex propagate(double w, double er, double d, int m, int n)
745 {
746     double kz;
747     complex gamma;
748
749     kz = sqr(w/v)*er - sqr(m*PI/d) - sqr(n*PI/d);
750     if( kz > 0 )
751     {
752         gamma = complex(0, sqrt(kz));
753         return( gamma );
754     }
755     else
756     {
757         gamma = complex(sqrt(-kz), 0);
758         return( gamma );
759     }
760 }
761
762
763 /*****************************************************************
764     imp_neg()
765
766     Computes the impedance seen looking in the negative direction
767     terminated in a mirror (short circuit).  The calculation is
768     general enough that an air gap and substrate between the
769     mirror are taken into account.
770
771 *****************************************************************/
772 void imp_neg(double w, double Er_subs, double d, double t, double l,
773             int FLIP, int m, int n, complex *zn_te, complex *zn_tm)
774 {
775     double factor;
776     complex gam_air, gam_subs, zn_te_gap, zn_tm_gap;
777     complex zn_te_subs0, zn_tm_subs0;
```

```
778
779 //  propagation constant of air
780     gam_air = propagate(w, Er_air, d, m, n);
781 //  propagation constant of substrate
782     gam_subs = propagate(w, Er_subs, d, m, n);
783
784 // compute the impedances looking in the negative direction
785 // with an air gap and the substrate in the path  to the mirror
786
787     zn_te_gap = z_te(gam_air, w) * xtanh(gam_air * l);
788     zn_tm_gap = z_tm(gam_air, w, Er_air) * xtanh(gam_air * l);
789
790 // FLIP = 1 means the dielectric faces free space
791     if (FLIP == 1)
792     {
793         *zn_te = zn_te_gap;
794         *zn_tm = zn_tm_gap;
795     }
796 // FLIP = 0 means the dielectric faces mirror
797     else
798     {
799         zn_te_subs0 = z_te(gam_subs, w);
800         zn_tm_subs0 = z_tm(gam_subs, w, Er_subs);
801
802         *zn_te = zn_te_subs0 * (zn_te_gap + zn_te_subs0
803                     * xtanh(gam_subs * t) );
804         *zn_te = *zn_te / ( zn_te_subs0 + zn_te_gap
805                     * xtanh(gam_subs * t) );
806
807         *zn_tm = zn_tm_subs0 * (zn_tm_gap + zn_tm_subs0
808                     * xtanh(gam_subs * t) );
809         *zn_tm = *zn_tm / ( zn_tm_subs0 + zn_tm_gap
810                     * xtanh(gam_subs * t) );
811     }
812 }
813
814
815 /******************************************************************
816     imp_plus()
817
818     Computes the impedance seen looking in the positive direction
819     terminated in free space (377ohm).  The calculation is
820     general enough that a substrate between free space
821     is allowed. (FLIP = 1)
822
823 ******************************************************************/
824 void imp_plus(double w, double Er_subs, double d, double t, int FLIP,
825               int m, int n, complex *zp_te, complex *zp_tm)
826 {
827     complex gam_air, gam_subs;
828     complex zp_te_subs0, zp_tm_subs0, zp_te_air, zp_tm_air;
829
830 //  propagation constant of air
```



```
831     gam_air = propagate(w, Er_air, d, m, n);
832
833 // FLIP = 1 means the dielectric faces free space
834     if (FLIP == 1)
835     {
836 //  propagation constant of substrate
837         gam_subs = propagate(w, Er_subs, d, m, n);
838
839         zp_te_air = z_te(gam_air, w);
840         zp_tm_air = z_tm(gam_air, w, Er_air);
841
842         zp_te_subs0 = z_te(gam_subs, w);
843         zp_tm_subs0 = z_tm(gam_subs, w, Er_subs);
844
845         *zp_te = zp_te_subs0 * (zp_te_air + zp_te_subs0
846                     * xtanh(gam_subs * t) );
847         *zp_te = *zp_te / ( zp_te_subs0 + zp_te_air
848                     * xtanh(gam_subs * t) );
849
850         *zp_tm = zp_tm_subs0 * (zp_tm_air + zp_tm_subs0
851                     * xtanh(gam_subs * t) );
852         *zp_tm = *zp_tm / ( zp_tm_subs0 + zp_tm_air
853                     * xtanh(gam_subs * t) );
854     }
855 // FLIP = 0 means the dielectric faces mirror
856     else
857     {
858         *zp_te = z_te(gam_air, w);
859         *zp_tm = z_tm(gam_air, w, Er_air);
860     }
861 }
862
863
864 /******************************************************************
865     sumterms()
866
867 ******************************************************************/
868 void sumterms(double w, double Er_subs, double d, double t, double l,
869               int FLIP, int MM, int NN, complex *zl, complex *yc,
870               complex *ytem)
871 {
872     int m, n;
873     double Kc, Kx, Ky, c_term, l_term, denom;
874     complex zn_te, zn_tm, zp_te, zp_tm, z_te, y_tm;
875
876     *zl = complex(0,0);
877     *yc = complex(0,0);
878
879     for(n=0; n<=NN; n++)
880     {
881         for(m=0; m<=MM; m++)
882         {
883             imp_neg(w,Er_subs,d,t,l,FLIP,m,n,&zn_te,&zn_tm);
```

```
884                 imp_plus(w,Er_subs,d,t,FLIP,m,n,&zp_te,&zp_tm);
885                 Kx = m*PI/d;
886                 Ky = n*PI/d;
887                 Kc = sqr(Kx) + sqr(Ky);
888
889 // For m=0 the TE mode contribution is zero and can be ignored
890                 if( m > 0 )
891                 {
892                     l_term = ep(0,n)*ep(m,0)/sqr(Kx)*Kc*C[m][n]*C[m][n];
893                     z_te = (zn_te*zp_te)/(zn_te + zp_te);
894                     *zl += l_term * z_te;
895                 }
896
897 // For n=0 the TM mode contribution is zero and can be ignored
898                 if( n > 0 )
899                 {
900                     c_term = 2*ep(0,m)/sqr(Ky)*Kc*C[n][m]*C[n][m];
901                     y_tm = (1/zn_tm) + (1/zp_tm);
902                     *yc +=  c_term * y_tm;
903                 }
904                 if( m==0 && n==0 )
905                 {
906                     *ytem = (1/zp_te) + (1/zn_te);
907                 }
908             }
909         }
910 }
```

About the Software

The diskette that accompanies this book contains an installation program that loads the applications discussed in Chapters 1 and 8. Source code, executable program files, and sample configuration or data files are included for both sets of applications. The source code listings for the ECM, XDIP, and BOWTIE programs are included in the appendices at the end of Chapters 1 and 8. Brief instructions about using the programs are included in the README file on the diskette.

DISK CONTENTS

The disk includes six installation program files and a README file that contains information about the programs. The installation program will install the following files to a directory on your hard disk:

FREQUEN directory
- README
- CHAP1 directory
  - ECM.EXE
  - ECM.FOR
  - ECM.OBJ
  - EIN.DAT

CHAP8 directory
- BOWTIE.CFG
- BOWTIE.CPP
- PWR1A.CFG
- XDIP.CPP

DOS directory
- BOWTIE.EXE
- XDIP.EXE

OS2 directory
- BOWTIE32.EXE
- XDIP32.EXE

HARDWARE AND SOFTWARE REQUIREMENTS

The program files can be installed and run on any IBM PC compatible computer with a hard disk and the math coprocessor. A system with DOS 3.1 or higher should be used for running the DOS-based programs. If you wish to compile the supplied source code, any standard ANSI C++ of FORTRAN compiler should be able to process the CPP and FOR files.

MAKING A BACKUP COPY

Before using the enclosed diskette, make a backup copy of the original. This backup is for personal use and will only be required in case of damage to the original. Any other use of the diskette violates copyright law. Assuming the floppy drive you will be using is drive A, please do the following:

1. Insert the original diskette included with the book into drive A.
2. At the A:〉 prompt, type DISKCOPY A: A: and press Return.

You will be prompted to place the source diskette into drive A.

3. Press Return and wait until you are prompted to place the target diskette in drive A.
4. Remove the original diskette and replace it with your blank backup diskette. Press Return. The backup will be completed.

INSTALLING THE DISKETTE FILES

To install the files included on the disk you will need approximately 520KB of free disk space on your hard drive. To install

1. Assuming you will be using the drive A as the floppy drive for your diskette, at the A:〉 prompt type INSTALL. You may A:INSTALL at the C:〉 prompt.
2. Follow the instructions displayed by the installation program. The default drive choice is C and the default installation directory is FREQUEN. At the end of the process, you will be given the opportunity to review the README file for information about the program files.

Index

Active grid array, 1,18,211–324
Adhesives, 203, 205
Alumina (Al_2O_3), 232
Aluminum gallium arsenide (AlGaAs), 224
Aluminum Nitride (AlN), 232
Antiseries biased diode (ABD), 225

Bandpass radome, 147–193
Beryllium oxide (BeO), 232
Beam control, 213–214
  amplitude, 214, 215
  high speed, 216
  polarization, 213
  reflection phase, 213
  transmission phase, 215
Beam control applications, 214–216
  beam focusing, 215
  beam steering, 215
  Dicke switch, 215
  imaging, 216
  frequency modulation, 214
  frequency tuning, 214
  pulsed radar, 215
Beam control array, 211–248
  bow-tie, 228
  characterization, 241
  fabrication, 234–235
  hybrid, 233
  measurement, 238–241
  packaging, 232
  parallel resonant, 229
  series resonant, 211, 227
  slot, 227
  square-loop, 228
  stacked, 229
  testing, 236–237
  thermal performance, 230–231
  truncated, 228
Beam control array theory, 216–221
  capacitive slot, 217
  faulty cells, 221
  grid capacitance, 217–220
  parasitic capacitance, 219
  plane-wave approximation, 220
  power handling, 220
  rectangular unit cell, 219
  substrate loss, 221
  waveguide equivalence, 220
Beam control techniques, 242
  AC/RF, 242
  DC, 242
  optical, 242
  quasi-optical, 243
Beam focusing, 213
Beam steering, 213, 291
Bessel functions, 40

Cascading techniques, 102–106
  equal periodicity, 103
  different periodicity, 103
  single mode, 105, 131
  system periodicity, 103
Cassini, 115–118, 124–144
Circular polarization, 114, 116
Coefficient of thermal expansion (CTE), 201–202, 232
Composite materials, 197
Computer codes, 22–25, 296–324
Corrugated surface, 68

Dielectric properties, 196

Electromotive force (EMF) method, 251–254, 279, 283–284

Electrical properties, 200
 fiber, 200–202
 polymeric resins, 202
Environment requirements, 200, 209
Epitaxial liftoff, 232
Fabrication, 197, 206–209
 grid, 206–209
 structure, 207–209
Fast Fourier transform, 40
Frequency selective surface (FSS), 1
 aperture element, 2, 16, 28, 68, 147–148
 dielectric loading effects, 7–9,124
 element type, 4, 35
  cross-dipole, 4, 37, 113
  dipole, 4, 37
  double ring (DR), 15, 125–131
  double square loop (DSL), 22, 131–143
  four-legged dipole, 4, 184
  grided-square-loop, 4, 22, 114, 118–124
  Jerusalem-cross, 4, 35, 38
  patch-aperture-patch, 68
  ring, 4, 6, 117, 125–131, 139–143
  square-loop, 4, 22, 80
  three-legged dipole, 4, 182
  tripole 4, 16–17
 high-pass, 1–2, 15
 lattice, 9, 32
 low-pass, 1–2, 125, 137
 multiple screen, 29, 48–55, 94–106, 118, 131, 137–143
 patch element, 2, 28
 single screen, 3–14, 27–58, 90–98, 118–124, 125–131, 134–137, 147–176
 testing, 13–14
FSS analysis, 11–13, 27–81, 87–110, 149–193
 basis function, 41,150
  entire-domain, 36
  rooftop, 41, 118
  subdomain, 41
 Conjugate gradient method, 12, 44–45, 88, 251
 edge condition, 34, 39, 72
 equivalent circuit model (ECM), 11, 260–262, 276
 finite-element method, 251, 284
 Floquet, 27, 31, 90, 150, 163
 Fourier, 30, 31, 150
 freestanding, 11, 22–25, 27
 Galerkin, 33
 integral equation method, 12, 30, 149
 mode matching, 12, 150
 relative convergence, 13, 36
FSS applications, 14–18
 beam splitter, 17
 frequency scanning, 17
 laser cavity mirror, 18
 microwave oven, 14
 radome, 16, 147–193
 solar energy filter, 17
 spatial filter, 16–17
 subreflector, 14–15, 113–144
 sun shield, 18

Gallium Arsenide (GaAS), 224
Grating lobe, 9, 99

Honeycomb, 199–206
 core, 205–206
  Kevlar, 205–206
  Korex, 205
  Nomex, 205–206
 facesheet, 199–205

Image, 98, 131
Impedance boundary condition, 40
Indium gallium arsenide (InGaAs), 230
Indium phosphide (InP), 235

Kapton, 203
k-space diagram, 99

Metal-enhanced semiconductor FET (MESFET), 222, 256–260
Metal-oxide semiconductor FET (MOSFET), 222
Method of moments, 12, 251, 284
Millimeter-wave, 249
Molecular-beam epitaxy (MBE), 234
Monolithic microwave integrated circuit (MMIC), 215
Multiband FSS, 113–145

Orbiting very long baseline interferometer (OVLBI), 114–116

Phased array, 1, 215
Piriodic structure, 1–294
p-i-n diode, 214, 221
Power combining, 249
 conventional, 249
 quasi-optical, 249–250
Quasi-optical efficiency, 242
Quasi-optical grid array, 249–296
 amplifier, 287–294
  failure, 294
  gain, 288, 290, 293
  multimode, 291, 293
  return loss, 288, 290

  unit cell, 290
 bow-tie, 279
 conversion loss, 276
 dynamic range, 272
 edge effects, 252
 electric wall, 252
 filter, 294
 heterodyne receiver, 294
 loop gain, 270
 magnetic wall, 252
 maximum power-added efficiency, 267
 maximally efficient power gain, 268
 mixer, 272–287
 multiplier, 294
 noise power, 273
 optimal load impedance, 267
 oscillator, 255–272
  bar-grid, 258–259
  planar-grid, 259–264
  power-grid, 264–272
 phase shifter, 294
 power handling, 272
 source-feedback, 263
 strip, 279
 thermal design, 264
 Third-order intercept point, 286
 third-order intermodulation (IMD_3), 276

Quasi-optical network analyzer, 288, 290
Quasi-optical Q switch, 243

Reaction integrals, 163, 188–193

Scattering matrix, 87–88, 96–102
 truncation, 96–99
  rule of thumb, 98–99
Scattering parameter, 88–96
 generalized, 91
 single-screen FSS, 90–95
 two-port system, 88
Schottky diode, 214
Silicon on insulator (SOI), 222
Slotted screen, 2, 16, 28, 68, 147–188
Spatial domain, 12, 42, 149
Spectral domain, 12, 42, 90
Strip grating, 17, 68, 99–102
Surface channel varactor, 227
Superlattice barrier, 224

T-factor, 153
Thermal stability, 202
Thick screen FSS, 3, 68–72, 147–176
 analysis, 68–72,149–173
  admittance matrix, 157
  basis function, 150
  equivalent problem, 149
  magnetic-field integral equation, 149
  tangential aperture field, 150
 antenna performance through, 173–176
 circular element, 164–173
  artificial puck plate (APP), 164–176
  iris-loaded, 165–176
  puck plate, 164–165
 geometry, 68–69, 148
 general properties, 186–187
 rectangular element, 68–69, 161–164

Thin-screen FSS, 3, 122–124, 176–186
 general properties, 186–187
 performance, 182–186
 single screen, 122–124, 179–181
 two-screen, 98–101, 109, 131, 137–143, 181
Tracking and data relay satellite system (TDRSS), 113
Transistor, 287
 channel temperature, 265
 differential-pair, 287, 289
 Field-effect (FET), 221
 heterojunction bipolar (HBT), 289
 High-electron-mobility (HEMT), 222
Transmission line model (TLM), 11, 260–263
Transverse electromagnetic (TEM), 252
Transverse electric (TE), 7, 116
Transverse magnetic (TM), 7, 116

Varactor diode, 222
 inductive, 229
 pseudomorphic, 224
Voyager, 15, 113

Wood's anomaly, 11